APJ Abdul Kalam Technological University

Cluster 4: Kottayam

M. Tech Program in Electronics & Communication Engineering

(VLSI & Embedded Systems)

Scheme of Instruction & Syllabus: 2015 Admissions

Compiled By

Rajiv Gandhi Institute of Technology, Kottayam

July 2015

APJ Abdul Kalam Technological University

(Kottayam Cluster)

M. Tech in Electronics and Communication Engineering (VLSI and Embedded Systems)

Scheme

Credit requirements : 65 credits (21+18+14+12)
Normal Duration : Regular: 4 semesters; External Registration: 6 semesters;
Maximum duration : Regular: 6 semesters; External Registration: 7 semesters.
Courses: Core Courses: Either 4 or 3 credit courses; Elective courses: All of 3 credits

ELIGIBILITY: B.Tech / B.E in Electronics and Communication engineering, or allied branches with strong focus in electronics engineering/Biomedical Engineering.

Allotment of credits and examination scheme:-

Semester 1 (Credits:21)

Exam Slot	Course No:	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	04EC6501	VLSI Technology	4-0-0	40	60	3	4
B	04EC6503	Advanced Digital Design	3-0-0	40	60	3	3
C	04EC6505	CMOS VLSI Design	3-0-0	40	60	3	3
D	04EC6507	Design with ARM Microcontrollers	3-0-0	40	60	3	3
E	04EC65XX	Elective-1	3-0-0	40	60	3	3
	04GN6001	Research Methodology	0-2-0	100	0	0	2
	04EC6591	Seminar	0-0-2	100	0	0	2
	04EC6593	Lab	0-0-2	100	0	0	1
		Total	22				21

**See List of Electives-I for slot E*

List of Elective - I Courses

Exam Slot	Course No.	Course Name
E	04 EC 6509	ASIC & FPGA
E	04 EC 6511	VLSI Design Automation
E	04 EC 6513	Embedded Network Controllers
E	04 EC 6515	Embedded Software Design

Semester 2 (Credits: 18)

Exam Slot	Course No:	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	04 EC 6502	Analog Integrated Circuits	3-0-0	40	60	3	3
B	04 EC 6504	Advanced CMOS VLSI	3-0-0	40	60	3	3
C	04 EC 6506	Embedded Operating Systems & RTOS	3-0-0	40	60	3	3
D	04 EC 65XX	Elective - 2	3-0-0	40	60	3	3
E	04 EC 65XX	Elective - 3	3-0-0	40	60	3	3
	04 EC 6592	Mini Project	0-0-4	100	0	0	2
	04 EC 6594	Lab	0-0-2	100	0	0	1
		Total	21				18

**See List of Electives -II for slot D* *^See List of Electives -III for slot E*

List of Elective - II Courses

Exam Slot	Course Code	Course Name
D	04 EC 6508	VLSI Testing
D	04 EC 6512	Introduction to MEMS
D	04 EC 6514	DSP Based System Design
D	04 EC 6516	Hardware Software Co- Design

List of Elective - III Courses

Exam Slot	Course Code	Course Name
E	04 EC 6518	VLSI Digital Signal Processing
E	04 EC 6522	Reconfigurable Computing
E	04 EC 6524	Embedded Control Systems
E	04 EC 6526	Electronic Packaging

Summer Break

Exam Slot	Course No:	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
NA	04 EC 7590	Industrial Training	0-0-4	NA	NA	NA	Pass /Fail
		Total	4				0

Semester 3 (Credits: 14)

Exam Slot	Course No:	Name	L- T - P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	04 EC 75XX	Elective - 4	3-0-0	40	60	3	3
B	04 EC 75XX	Elective - 5	3-0-0	40	60	3	3
	04 EC 7591	Seminar II	0-0-2	100	0	0	2
	04 EC 7593	Project (Phase 1)	0-0-12	50	0	0	6
		Total	20				14

**See List of Electives-IV for slot A* *^See List of Electives-V for slot B*

List of Elective - IV Courses

Exam Slot	Course Code	Course Name
A	04 EC 7501	Mixed VLSI Circuits Design
A	04 EC 7503	System On Chip
A	04 EC 7505	Computer Architecture And Parallel Processing
A	04 EC 7507	Electronic System Design

List of Elective - V Courses

Exam Slot	Course Code	Course Name
B	04 EC 7509	High speed Digital Design
B	04 EC 7511	NANO Devices and Circuits
B	04 EC 7513	Power Management of Embedded Systems
B	04 EC 7515	VLSI For Wireless Communication

Semester 4 (Credits: 12)

Exam Slot	Course No:	Name	L- T - P	Internal Marks	External Evaluation Marks		Credits
NA	04 EC 7594	Project (Phase -II)	0-0-21	70	30	NA	12
		Total	21				12

Total: 65

SEMESTER I

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6501	VLSI TECHNOLOGY	4-0-0:4	2015

Pre-requisites: nil

Course Objectives:

- A study of fabrication processes used in VLSI
- Familiarise MOSFET principles in detail
- A study of monolithic Integrated circuits

Syllabus

Production of metallurgical and electronic grade silicon.Crystal and wafer preparation.Lithographic techniques.Etching, chemical vapour deposition and ion implantation.Carrier generation and recombination. Calculation of charge densities and position of Fermi level in semiconductors. Invariance of Fermi level at thermal and electrical equilibrium.Density variation of injected carriers in p-n junctions.One-sided and two-sided p-n junctions.Metal-semiconductor junctions and ohmic contacts. BJTs. Calculation of threshold voltage of MOSFETs. Expression for drain current of MOSFETs.Body effect.Circuit model of MOSFETs including body effect. Unloaded voltage gain of MOSFETs. Isolation of components.scaling.Tunneling currents.Transit time limitation of frequency response.

Course Outcome:

The student will be able to:

1. Explain fabrication process in VLSI.
2. Design New MOSFET Devices.
3. Design Monolithic Integrated Circuits.

Text Books:

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, Silicon VLSI Technology, Pearson Education, 2001
2. Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 5th Ed., Oxford University Press, 2004.

References:

1. Wolf S. and Tauber, R.N., Silicon Processing for the VLSI Era, Lattice Press, Sunset Beach, 2000.
2. Jaeger, R.C., Introduction to Microelectronic Processing,
3. Jacob Millman and Christos C. Halkias, Integrated Electronics, Tata McGraw-Hill
4. Sze, S.M., Physics of Semiconductor Devices, John Wiley and Sons, 3rd Ed.
5. Ben G. Streetman and Sanjay Kumar Banerjee Solid State Electronic devices, 6th Ed., Prentice-Hall of India, 2006.
6. Sorab K Gandhi, VLSI Fabrication Principles, John Wiley & Sons, New York, 1994
7. Nandita Das Gupta and Amitava Das Gupta, Semiconductor Devices, Prentice-Hall of India, 2004.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6501	**VLSI TECHNOLOGY**	**4-0-0:4**	
MODULES		**Contact Hours**	**Sem. Exam Marks (%)**
MODULE 1: Production of metallurgical grade silicon. Zone refining and Float zone refining methods to obtain electronic grade silicon. Czochralsky technique of crystal growth. Wafer preparation. Oxidation methods. Lithographic techniques. Contact, proximity and projection printing methods. Dependence of "feature size" on lithographic technique. Electron beam lithography. De Broglie wavelength. Etching methods. Chemical vapour deposition techniques. Epitaxial growth. Ion implantation techniques. Magnetic field deflection method for removal of unwanted ions. Metallisation.		10	15
MODULE 2: Carrier generation and recombination. Photons and phonons. Direct and indirect band gap materials and recombination mechanism in each. Calculation of charge densities using density of states function and Fermi-Dirac probability function. Proof for complete ionization of dopants at room temperature [9, p22]. Calculation of position of Fermi level. Proof for invariance of Fermi level in a system at thermal and electrical equilibrium [7, p108].		10	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: P-N junctions. Density variation of injected carriers in a p-n junction as a function of distance. Diode equation. Analysis of one-sided and double-sided p-n junctions. Calculation of diffusion and transition capacitances. Metal semiconductor junctions (Schottky diodes) and method of converting the metal semiconductor junction into an ohmic contact [6]. BJTs. Characteristic equation of the BJT. Early voltage		9	15
MODULE 4: Advantages of using MOSFETs as the active device in VLSI design. Structure of MOSFET and principle of operation. Ideal MOS structure. Calculation of threshold voltage for the ideal MOS structure. Modification of threshold voltage for non-ideal MOS structures [6]. Analysis to obtain drain current as a function of gate-to-source voltage. Channel length modulation and Early voltage. Calculation of g_m and r_o. Substrate bias effect (Body effect). Transconductancedue to body effect.		9	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Low frequency circuit model of MOSFET including body effect. Calculation of capacitances associated with MOSFETs. Complete all frequency model of MOSFET [2]. Calculation of unloaded voltage gain $\mu = g_m r_o$. Dependence of		9	20

unloaded voltage gain μ on drain current. Use of MOSFET circuit model in analysis.		
MODULE 6: Isolation of components. Junction isolation and dielectric isolation. Techniques for modifying threshold voltage. Silicon gate technology. Advantages of scaling. Scaling of oxide thickness to reduce threshold voltage. Problem of tunnelling current in thin oxide layers. Tunnelling mechanism and its quantification. Techniques to reduce tunnelling. Velocity saturation. Transit time limitation of frequency response and need to reduce channel length . Resistors and capacitors.	9	20
END SEMESTER EXAM		

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6503	ADVANCED DIGITAL DESIGN	3-0-3:3	2015

Pre-requisites: nil

Course Objectives:

- A detailed study of combinational & sequential circuits
- Familiarise with asynchronous sequential circuits
- A brief knowledge on RTL design of data path components and controller

Syllabus

Review of Boolean Algebra-Shannon's Expansion Theorem, Consensus Theorem, Reed Muller Expansion, A detailed study of combinational & sequential circuits-design; Clock skew and Jitter; Familiarise asynchronous sequential circuits ; Static ,dynamic and essential hazards;Designing with SM charts ;A brief knowledge on RTL design of data path components and controller; overview of Optimizations and Trade-offs ; Design Using Hardware Description Languages

Course Outcome:

The student will be able to:

1. Design combinational and sequential logic circuit and describe them using Hardware description Language.
2. Analyse and Design Asynchronous sequential circuits.
3. Design elementary data paths and control unit for processors.
4. Estimate and compute the area, delay and power consumption of logic circuit.

Text Books:

1. Charles H.Roth,Jr, "Fundamentals of Digital Design", PWS Pub.Co.,1998.
2. Kenneth J Breeding "Digital Design Fundamentals", , Prentice Hall,.1989.
3. Frank Vahid, Digital Design (Preview Edition), Wiely India Edition,2012.

References:

1. John F. Wakerly , "Digital Design Principles and Practices", 4/e, Prentice Hall, 2005
2. William I. Fletcher "A Systematic Approach to Digital Design", PHI, 1996.
3. James E. Palmer, David E. Perlman "Introduction to Digital Design", Tata McGraw Hill, 1996.
4. S.Devadas, A.Ghosh and K.Keutzer "Logic Synthesis",McGraw Hill, 1994.
5. N.N Biswas "Logic Design Theory",Prentice Hall of India, 1st Edn,1993.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6503	**ADVANCED DIGITAL DESIGN**	**3-0-0:3**	
MODULES		**Contact Hours**	**Sem. Exam Marks (%)**
MODULE 1: Review of Boolean Algebra-Shannon's Expansion Theorem, Consensus Theorem, Reed Muller Expansion, Combinational-Circuit design using Programmed Minimization Methods.Sequential Circuit Design: Mealy and Moore machines, Finite State Machine design procedure – derive state diagrams; obtain state tables, state reduction methods, and state assignments. Clock skew and Jitter. Combinational Logic & Sequential Logic Description Using Hardware Description Languages.		9	15
MODULE 2: Asynchronous sequential circuits: Derivation of excitation table, Race conditions and cycles, Static and dynamic hazards, Methods for avoiding races and hazards, essential hazards, Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts.		9	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Data path Components: Registers, Adder, Comparators, Multiplier—Array-Style, Subtractors and Signed Number, Arithmetic-Logic Units—ALUs, Shifters, Counters and Timers, Register Files. Data path Component Description Using Hardware Description Languages.		7	15
MODULE 4: Controller Design: FSM based Controller design, Micro programmed Controllers		5	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: RTL Design: High-Level State Machine, RTL Design Process. Behavioural-Level Design: C to Gates, Hierarchy—A Key Design Concept. Determining Clock Frequency.		6	20
MODULE 6: Optimizations and Tradeoffs: Combinational Logic Optimizations and Tradeoffs, Sequential Logic Optimizations and Tradeoffs, Data path Component Tradeoffs, RTL Design Optimizations and Tradeoffs.RTL Design Using Hardware Description Languages		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6505	CMOS VLSI DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To understand the basic MOS inverter and its characteristics
- To outline the performance parameters of CMOS circuits
- To discuss the various combinational and sequential CMOS circuits
- To explain the static and dynamic logic circuits

Syllabus

To understand the basic MOS inverter and its characteristics; outline the performance parameters of CMOS circuits; discuss the various combinational and sequential CMOS circuits; explain the static and dynamic logic circuits

Course Outcome:

The student will be able to:

1. Understand various parameters involved in CMOS circuit design
2. Design various combinational and sequential CMOS circuits

Text Books:

1. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits-Analysis and Design”, 3/e, Tata McGraw-Hill Education, 2003.
2. Neil H. E. Weste and David Money Harris, “CMOS VLSI Design - A Circuits and Systems Perspective”, 4/e, Pearson Education, 2011

References:

1. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2/e, Pearson Education.
2. R. Jacob Baker, Harry W. Li, David E. Boyce, “CMOS, Circuit Design, Layout, and Simulation”, 3/e, Wiley Interscience.
3. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6505	CMOS VLSI DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: **The MOS Inverter**: Principle, Depletion and enhancement load inverters ,The basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behaviour Propagation Delay, Power Consumption, Latch-up in CMOS circuits, Tristate inverter, BiCMOS inverter.		9	15
MODULE 2: **Performance parameters:** Static, dynamic and short circuit power dissipations; Propagation delay; Power delay product; Fan in, fan out and dependencies. Delay Estimation: RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay , Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks Interconnect: Resistance, Capacitance, Delay, Crosstalk		9	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: **Combinational MOS Logic Circuits:** MOS logic circuits with NMOS loads Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design –Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OAI gates.		7	15
MODULE 4: **Sequential MOS Logic Circuits:** Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.		5	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: **Static Logic Circuits:** Pseudo-NMOS – Full complementary CMOS, Ratioed logic, Pass Transistor logic Pass transistor Logic (PTL) families: DPTL, CPTL - DCVS, CMOS transmission gates, Designing with Transmission gates.		6	20
MODULE 6: **DynamicLogic Circuits:** Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic High performance Dynamic CMOS circuits, N-P Dynamic logic - Domino logic - NORA logic - TSPC logic - Multiple output Domino logic - Dynamic NORA		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6507	DESIGN WITH ARM MICROCONTROLLER	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- Thorough understanding of embedded systems, its design requirements, architecture
- Embedded system Project design techniques
- ARM processor architecture, its programming and about various software tools for the embedded system design especially ARM

Syllabus

Asystem engineering approach to embedded systems; embedded systems hardware point of view; Integrated Development environment and hardware simulator; ARM architecture and features; Programming the ARM processor; ARM instruction sets; ARM assembly Programs; Programming ARM MCU using C.

Course Outcome:

The student will be able to:
1. Understand the design requirements and architecture of embedded systems
2. Design Embedded system projects
3. Program ARM Microcontroller

Text Books:

1. Tammy Noergaard. Embedded Systems Architecture ,Elsevier, 2011
2. Lyla B Das, Embedded Systems - An Integrated Approach, Pearson, 2012.

References:

1. Steve Furber,ARM System - on - Chip Architecture,Pearson,2nd edition.
2. Andrew N. Sloss,DominicSymes and Chris Wright, ARM System Developer's Guide - Designing and Optimizing Systemsoftware, Elsevier,2006
3. ARM Company Ltd. "ARM920T Technical Reference Manual (Rev 1) - ARM DDI0151C".

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6507	DESIGN WITH ARM MICROCONTROLLER	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: A system engineering approach to embedded systems - Introduction and definition of Embedded Systems ,Embedded System Design, Introduction and importance of embedded systems architecture, the embedded systems Model. Microprocessor Vs microcontroller, Classification of MCUs		6	15
MODULE 2: Embedded systems - The hardware point of view- MCU, memory, low power design Sensors, ADCs and actuators.		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: The integrated Development Environment (IDE) Conversion steps from source file to an executable file and downloading the Hex file to the Non-volatile memory Hardware simulator		6	15
MODULE 4: History of ARM, The ARM Core, features of ARM ARM architecture versions, ARM architecture ARM920T Core Processor Functional Block Diagram Programming the ARM processor. The ARM memory interface The Advanced Microcontroller Bus Architecture (AMBA).		9	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: ARM instruction sets General structure of an assembly language line. Writing ARM assembly Programs		8	20
MODULE 6: Peripheral programming of ARM MCU using Internal block diagram of LPC2148: Timer Peripheral programming of ARM MCU using Internal block diagram of LPC2148: PWM and UART		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6509	ASIC&FPGA	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

Syllabus

Types of ASICs and different approaches for design of ASIC, Memory technologies; programmable ASICs- Programmable ASIC logic cells, Programmable ASIC I/O cells; FPGA architecture; Design of FPGA based systems using low level tools ; physical design of ASIC based systems; Physical design- partitioning ,Floor planning, Placement, Routing, Circuit extraction and DRC.

Course Outcome:

The student will be able to:
1. Understand different types of ASICs and different approaches for design of ASIC
2. Understand programmable ASICs and different types of Programmable ASICs
3. Understand different FPGA architecture
4. Design of FPGA based systems using low level tools
5. Apply different types of tools for the physical design of ASIC based systems

Text Books:

1. M.J.S. Smith, Application Specific Integrated Circuits, Pearson Education, 2008

References:

1. S. Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 1994.
2. John V. Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 1995.
3. P. K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
4. P. K. Lala, Digital System Design using Programmable Logic Devices , BSP, 2003

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6509	ASIC&FPGA	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Types of ASICs, Design Flow.ASIC Cell Library, Combinational Logic Cell, Sequential Logic Cell, Data-path Logic Cell, Library Cell design,Gate Array Design, Standard Cell design, Data path Cell design.		8	15
MODULE 2: The anti-fuse, SRAM, EPROM and EEPROM technologies, PREP benchmarks. Programmable ASIC logic cells – ACTEL ACT, XILINX LCA, ALTERA FLEX, ALTERA MAX, Programmable ASIC IO Cells - AC & DC Input & Output, Clock & Power input.		8	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000, Altera MAX 7000, Altera MAX 9000, Altera FLEX.		7	15
MODULE 4: Design systems, Logic Synthesis, Schematic entry, Low level design language.PLA tools, EDIF, CFI design representation		6	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Physical design, CAD tools. System partitioning, FPGA partitioning, partitioning methods.		6	20
MODULE 6: Floor planning, Placement, Routing- Global routing, detailed routing, special routing. Circuit extraction and DRC		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6511	VLSI DESIGN AUTOMATION	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- The study of basic and advanced algorithms used for VLSI CAD tools
- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis of digital Very Large Scale Integration (VLSI) systems.

Syllabus

Data structures for Representation of Graphs;Introduction to combinational logic synthesis, Binary Decision Diagram; Hardware models for High-level synthesis.Allocation , assignment and scheduling; Compaction: Problem formulation & types; Partitioning: Problem formulation & algorithms; Placement, floor planning & pin assignment: Problem formulation and algorithms; Global Routing: Problem formulation, classification of global routing algorithms, Detailed routing: Problem formulation and classifications.

Course Outcome:

The student will be able to:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design
2. Demonstrate knowledge and understanding of fundamental concepts in CAD.
3. Demonstrate knowledge of computational and optimization algorithms and tools applicable to solving CAD related problems.
4. Establish capability for CAD tool development and enhancement.

Text Books:

1. Gerez, Sabih H. Algorithms for VLSI design automation. Vol. 8. New York: Wiley, 1999.
2. Sherwani, Naveed A. Algorithms for VLSI physical design automation. Springer Science & Business Media, 2012.

References:

1. Meinel, Christoph, and Thorsten Theobald. Algorithms and data structures in VLSI design: OBDD-foundations and applications. Springer Science & Business Media, 2012.
2. Drechsler, Rolf. Evolutionary algorithms for VLSI CAD. Springer Science & Business Media, 2013.
3. Trimberger, Stephen M. An Introduction to CAD for VLSI. Springer Science & Business Media, 2012. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "C. Stein Introduction to Algorithms." MIT Press 5.3 (2001): 55.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6511	VLSI DESIGN AUTOMATION	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Data structures for Representation of Graphs , Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's and Bellman Fort Algorithm for single pair Shortest paths, Floyd-Warshall algorithm for All pair Shortest path, Matrix multiplication modelling of All pairs shortest path problem, Min cut and Max cut Algorithms		8	15
MODULE 2: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis. Allocation , assignment and scheduling		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Compaction: Problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction, Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms		7	15
MODULE 4: Placement, floor planning & pin assignment: Problem formulation, Placement algorithms, Floor planning concepts, Constraint based floor planning, Floor planning algorithms for mixed block & cell design, General & channel pin assignment		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches		7	20
MODULE 6: Detailed routing: Problem formulation, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms , Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6513	EMBEDDED NETWORK CONTROLLERS	3-0-0:3	2015

Pre-requisites: nil

Course Objective:

To understand the concepts of different communication protocols and its implementation.

Syllabus

Introduction to Embedded Networking,: Serial communication protocols: PC Parallel port programming: USB bus: USB bus communication: Microcontroller USB Interface: CAN Bus: PIC microcontroller CAN Interface: Micro CAN: Elements of a network:, Design choices: Inside the Internet protocol: Wireless Embedded Networking

Course Outcome:

The student will be able to:

1. Understand the CAN protocol and its Implementation
2. Understand the Serial and Parallel Communication Protocol including USB

Text Books:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Embedded System Academy 2005.

References:

1. Dogan Ibrahim, ‘Advanced PIC microcontroller projects in C’, Elsevier 2008
2. Mohammad Farsi, Manuel Bernardo Barbosa, “CANopen: Implementation Made Simple”, Research Studies Press,1999.
3. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications
4. BhaskarKrishnamachari, ‘Networking wireless sensors’, Cambridge press 20055.
5. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6513	EMBEDDED NETWORK CONTROLLERS	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction to Embedded Networking, Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485, Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C)		6	15
MODULE 2: PC Parallel port programming -ISA/PCI Bus protocols –Firewire, USB bus – Introduction – Speed Identification on the bus – USB States, USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs, CAN Bus – Introduction - Frames – Bit stuffing –Types of errors – Nominal Bit Timing		8	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: PIC microcontroller CAN Interface –A simple application with CAN, Micro CAN-Implementing CAN open Communication layout and requirements – Comparison of implementation methods, Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.		8	15
MODULE 4: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed, Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications		6	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Inside the Internet protocol-embedded Ethernet- Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input, Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.		6	20
MODULE 6: Wireless Embedded Networking- Wireless sensor networks – Introduction – Applications, Network Topology – Localization – Time Synchronization, Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6515	EMBEDDED SOFTWARE DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- Discuss about embedded software development tools and embedded program development.
- A brief insight in to the embedded operating system and its various design perspectives followed by OS performance guidelines.
- Familiarise various device drivers and computer software development.

Syllabus

Embedded software development tools:Embedded program development,Embedded Firmware Design and Development,Software Design Aspects:Embedded Operating Systems,Device Dependent Software:DeviceDrivers,Introduction to middleware and application software.

Course Outcome:

The student will be able to get familiarised with embedded operating system and various device drivers and computer software development.

Text Books:

1. Lyla B Das, —Embedded Systems –An Integrated Approach, Pearson 2012.
2. Shibu K V, —Introduction to Embedded Systems, McGraw Hills 2010.
3. Tammy Noergaard, —Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers, Elsevier, 2/e, 2010.

References:

1. Qing Li & Caroline Yao, —Real-Time Concepts for Embedded Systems, CMP Books, 2003.
2. David E Simon, —An Embedded Software Primer, Addison -Wesley, 2006.
3. Raj Kamal, —Embedded Systems: Architecture, Programming and Design, McGraw Hill, 2008.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6515	EMBEDDED SOFTWARE DESIGN	3-0-0:3	
MODULES		**Contact Hours**	**Sem. Exam Marks (%)**
MODULE 1: **Embedded software development tools**: Embedded program development: Initial Steps, the Integrated Development Environment: Code editor-Builder-Simulator-GUI, Downloading the Hex file to the Non-volatile Memory: Out of circuit programming, In System Programming (ISP), Hardware Simulator.		7	15
MODULE 2: **Embedded Firmware Design and Development**: Embedded Firmware Design Approaches Embedded Firmware Development Languages.		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: **Software Design Aspects**: Embedded Operating Systems: Layers of an Operating System, History of Operating System, Functions Performed by an Operating System: Process, Multitasking and Process Management Process Implementation—Process Scheduling-Inter task communication.		7	15
MODULE 4: **Embedded Operating Systems continued**: Memory management-User memory space – Kernel memory space I/O and File system managements Standards-POSIX (Portable Operating System Interface) OS performance Guidelines, OSes and Board Support Packages.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: **Device Dependent Software**: Device Drivers: Definition, Purpose of a device driver, Device Drivers for Interrupt Handling Memory Device Drivers, On-Board Bus Device Drivers, and Board I/O Driver Examples confined to initialization of Ethernet and RS 232.		7	20

MODULE 6: **Introduction to middleware and application software**: **Middleware**: Definition, Middleware Examples - Networking Middleware Driver Examples-Internet Layer Middleware (Internet Protocol) -Transport Layer Middleware (User Datagram Protocol). **Application Software**: Application Layer Software Examples - File Transfer Protocol (FTP) Client Application, Simple Mail Transfer Protocol (SMTP) and E-Mail Hypertext Transfer Protocol (HTTP)	7	20
END SEMESTER EXAM		

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 GN 6001	RESEARCH METHODOLOGY	0-2-0:2	2015

Pre-requisites: nil

Course Objectives:

- To get introduced to research philosophy and processes in general.
- To formulate the research problem and prepare research plan
- To apply various numerical /quantitative techniques for data analysis
- To communicate the research findings effectively

Syllabus

Introduction to the Concepts of Research Methodology, Research Proposals, Research Design, Data Collection and Analysis, Quantitative Techniques and Mathematical Modeling, Report Writing

Course Outcome:

The student will be able to:
1. apply the basic aspects of the Research methodology, to formulate a research problem and its plan
2. deploy numerical/quantiative techniques for data analysis.
3. have good technical writing and presentation skills.

Text Books:

1. Research Methodology: Methods and Techniques', by Dr. C. R. Kothari, New Age International Publisher, 2004
2. Research Methodology: A Step by Step Guide for Beginners' by Ranjit Kumar, SAGE Publications Ltd; Third Edition

References:

1. Research Methodology: An Introduction for Science & Engineering Students', by Stuart Melville and Wayne Goddard, Juta and Company Ltd, 2004
2. Research Methodology: An Introduction' by Wayne Goddard and Stuart Melville, Juta and Company Ltd, 2004
3. Research Methodology, G.C. Ramamurthy, Dream Tech Press, New Delhi
4. Management Research Methodology' by K. N. Krishnaswamy et al, Person Education.

OURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 GN 6001	RESEARCH METHODOLOGY	0-2-0:2	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction to Research Methodology, Concepts of Research, Meaning and Objectives of Research, Research Process, Types of Research, Type of research: Descriptive vs. Analytical, Applied vs. Fundamental, Quantitative vs. Qualitative, and Conceptual vs. Empirical.		5	15
MODULE 2: Criteria of Good Research, Research Problem, Selection of a problem, Techniques involved in definition of a problem, Research Proposals – Types, contents, Ethical aspects, IPR issues like patenting, copyrights.		4	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Meaning, Need and Types of research design, Literature Survey and Review, Identifying gap areas from literature review, Research Design Process, Sampling fundamentals, Measurement and scaling techniques, Data Collection – concept, types and methods, Design of Experiments.		5	15
MODULE 4: Probability distributions, Fundamentals of Statistical analysis, Data Analysis with Statistical Packages, Multivariate methods, Concepts of correlation and regression, Fundamentals of time series analysis and spectral analysis		5	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: **Report Writing:** Principles of Thesis Writing, Guidelines for writing reports & papers, Methods of giving references and appendices, Reproduction of published material, Plagiarism, Citation and acknowledgement		5	20
MODULE 6: Documentation and presentation tools – LATEX, Office Software with basic presentations skills, Use of Internet and advanced search techniques		4	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6591	**SEMINAR I**	**0-0-2:2**	**2015**

COURSE CONTENT

Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the first semester of the M. Tech. Programme. He / she shall select the topic based on the References: from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6593	DESIGN LAB-I	0-0-2:1	2015

Course Objectives:

To experiment the concepts introduced in the core and elective courses offered in the first semester with the help of simulation tools and related hardware

Course Outcome:

The student will be able to design &analyze sequential and combinational circuits in CMOS

	COURSE CONTENT	HRS
	Tools: CADENCE/SYNOPSYS/MENTOR GRAPHICS or any other equivalent tools	
VLSI EXPERIMENTS	**Experiments:** **PART A** **Simulation and Synthesis of Digital Circuits** **(Synthesis – Use Library 180nm or less)** 1. Experiments on combinational circuits 2. Experiments on Sequential Circuits 3. Experiments based on FSM Machines	6
	PART B **Design (Schematic), Simulation and Characterization of the following CMOS Logic Circuits** **(Technology Library 180nm or less)** 1. Inverter 2. NAND 3. NOR 4. Adders 5. Flip-Flops	10
	Tools and Boards: Any other equivalent tools	
Embedded Experiments	Embedded Processor /Controller based experiments to be done on a 32 bit Processor/Controller based on IDE and Boards Peripheral Interfacing based experiments (serial/parallel port based) IDE based simulations	12

SEMESTER II

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6502	ANALOG INTEGRATED CIRCUITS DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- The study of basic and advanced MOS amplifier configurations, their biasing circuit elements and evaluation of performance matrices
- Develop an understanding of device and circuit theory sufficient to estimate the low and high frequency behaviour of linear circuits, including noise
- To lay good foundation on the design and analysis of CMOS analog integrated circuits.

Syllabus

Single stage amplifiers - Basic configurations; Current Mirrors and Voltage references-types and analysis, Layout and packaging consideration for analog circuits – design rules, Multi finger transistors – substrate coupling ; Differential amplifiers ;Output stages : source follower as an output stage, CMOS Class AB output stages Frequency response of Amplifiers and noise- Statistical Characteristics of Noise , Noise Spectrum, Amplitude Distribution ,Correlated and Uncorrelated Sources

Course Outcome:

The student will be able to:
1. Analyze and design current sources/sinks/mirrors
2. Analyze characteristics of single-stage amplifiers and differential amplifiers
3. Understand the importance of noise and distortion in analog circuits

Text Books:

1. R.J. Baker, H.W. Li, D.E. Boyce. CMOS. Circuit design, Layout, and Simulation (2nd Edition), 2005. 1038p.
2. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill 2008

References:

1. Gray, Hurst, Lewis, Meyer, “Analysis and Design of Analog Integrated Circuits”, 5th Edition, Wiely India,2010
2. Philip E Allen, Douglas R Holberg, “CMOS Analog Circuit Design”, International Student(Second) Edition, First Indian Edition 2010
3. T.C Carusone, David A. Johns, Kenneth W.Martin“Analog Integrated Circuit Design”,2nd Edition, Wiley.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6502	ANALOG INTEGRATED CIRCUITS DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: **Single stage amplifiers:**Basic configurations**:** common source amplifier-Resistive load, Diode Connected load, Current Source load, common drain amplifiers - common gate amplifiers,Cascodeamplifiersand folded cascode amplifiers.		8	15
MODULE 2: **Current Mirrors:** Simple CMOS current mirror ,Sensitivity analysis - Temperature analysis -Transient response, Cascode current mirror - Wilson current mirror		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: **Voltage references:** Supply independent and temperature independent references-Band gap references, PTAT current generation and constant Gm biasing, Layout and packaging consideration for analog circuits – design rules, Multi finger transistors – substrate coupling		7	15
MODULE 4: **Differential amplifiers:** Source coupled pair: current source load – CMRR – Matching considerations, Source cross coupled pair, cascode loads**,** Wide swing differential amplifiers: – constant transconductance differential amplifier,Current differential amplifier Output stages **:** source follower as an output stage, CMOS Class AB output stages		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: **Frequency response of Amplifiers:** General Considerations **–** Miller effect – Association of Poles with Nodes, Common source, Source followers, Common gate, Cascode stage, Differential Pair		7	20
MODULE 6: **Noise** Statistical Characteristics of Noise - Noise Spectrum, Amplitude Distribution - Correlated and Uncorrelated Sources		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6504	ADVANCED CMOS VLSI	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To know the various sources of power dissipation in CMOS circuits
- To understand the various low voltage circuit techniques for leakage power reduction
- To study the various low voltage circuit design of static and dynamic CMOS circuits

Syllabus

Physics of Power dissipation in MOSFET devices-MIS structure; Sources of Power dissipation in CMOS-static and active power dissipation ;Transistor leakage mechanisms of deep submicron transistors; Circuit techniques for leakage power reduction ; Submicron device design issues; Low voltage circuit design techniques; Low-Voltage Low –Power Circuit design style, Non clocked logic-CMOS Static logic Circuits; Clocked logic family-Basic concept; Organization of static RAM

Course Outcome:

The student will be able to:
1. Identify the sources of power dissipation of various digital circuits
2. Understand the leakage source and reduction techniques
3. Design low power adders, multiplexers and low power memory

Text Books:

1. Kaushik Roy, Sharat C Prasad, Low power CMOS VLSI circuit design, Wiley India
2. Low voltage CMOS VlSI-James .B.Kuo,Jea Hong Lou
3. KiatSeng Yeo, Kaushik Roy, Low voltage, low power VLSI sub systems, Tata McGraw Hill

References:

1. Anatha P Chandrakasan, Robert W Brodersen, Low power digital CMOS Design, Kluwer Academic
2. GrayYeap, Practical low power digital VLSI design, Springer
3. Christian Piguet, Low power CMOS circuits, Taylor & Francis
4. AbdellatifBellaouar, Mohamed I Elmasry, Low power digital VLSI design, Kluwer

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6504	ADVANCED CMOS VLSI	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Physics of Power dissipation in MOSFET devices-MIS structure-threshold voltage-body effects-short channel and narrow width effects –sub threshold current , Sources of Power dissipation in CMOS-static and active power dissipation Transistor leakage mechanisms of deep submicron transistors		8	15
MODULE 2: Why low voltage CMOS, Side effects of Low –Voltage, Circuit techniques for leakage power reduction – standby leakage control using transistor stacks, multiple Vth techniques, Dynamic Vth techniques, supply voltage scaling technique		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Submicron device design issues, Minimizing short channel effect , Low voltage circuit design techniques, Low-Voltage Low –Power Circuit design style, Non clocked logic-CMOS Static logic Circuits, Difficulties for Low-Power and Low –Voltage operation		7	15
MODULE 4: CMOS differential static logic-DCVS-DSL-DCVSPG, CMOS pass transistor logic, BiCMOS static Logic Circuit-Sub-3V BiCMOS-1.5 V BiCMOS logic with transient feedback, adiabatic logic -1.5 V CMOS energy efficient logic circuit		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Clocked logic family-Basic concept, Domino logic(domino NAND gate), Differential Current Switch Logic, NORA logic		7	20
MODULE 6: Organization of static RAM, MOS static RAM cell, Banked organization of SRAMs, Low voltage low power (LVLP) SRAM cell Designs		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6506	EMBEDDED OPERATING SYSTEMS & RTOS	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To study in detail, learn implementation aspects of real time systems and to make a case study
- To familiarize with the fundamentals of Embedded Systems and basic operating system concepts,
- To learn implementation aspects of real time systems and to make a case study

Syllabus

Introduction to embedded systems; Operating Systems -Basic Principles and Operating System structures ; Scheduling algorithms and Introduction to RTOS

Course Outcome:

The student will be able to:
1. Get an Idea about the Real Time Embedded Systems
2. Get Familiarize with the Real Time Operating Systems

Text Books:

1. Raj Kamal, Introduction to Embedded Systems, Tata McGraw Hill Publications, 2002.
2. Frank Vahid,Tony D. Givargis, Embedded System Design- A Unified Hardware/ Software Introduction, John Wiley and Sons, Inc 2002

References:

1. Tammy Noergaard. Embedded Systems Architecture ,Elsevier, 2011
2. Programming for embedded systems, Dreamtech Software Team, Wiley, 2002
3. Silberschatz,Galvin,Gagne" Operating System Concepts, 6thed,John Wiley,2003
4. Real-Time Concepts for Embedded Systems by Qing Li, Caroline Yao, CMP Books.
5. VxWorks Reference Manual

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6506	EMBEDDED OPERATING SYSTEMS & RTOS	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction to embedded systems: Classification of embedded systems, overview of embedded system architecture. Hardware Architecture, Embedded Software Development Process, Embedded Systems on a Chip (SoC).		6	15
MODULE 2: Operating Systems: Basic Principles-Operating System structures :System Calls, Files. Processes –Design and Implementation of processes, Communication between processes Introduction to Distributed operating system –issues in distributed system: states, events, clocks. Distributed scheduling - Fault & recovery		8	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Scheduling algorithms and Introduction to RTOS: Scheduling algorithms: Round Robin, Pre-emptive Earliest deadline first. RTOS Architecture, Introduction to RTOS- Task and task states, Task and data, Semaphore and shared data,		7	15
MODULE 4: Inter task communication and synchronization- Semaphore, Message Queues, Mail boxes and pipes. Timer functions , events, Memory Management, Interrupt routine in an RTOS environment.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Case Studies: VxWorks Scheduling and Task Management –Real time scheduling Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts and I/O systems.		8	20
MODULE 6: OS Standards-POSIX(Portable Operating System Interface), OS Performance Guidelines. OSes and Board Support Packages (BSPs). Overview of linkers & linking process,Executable and linking format,Mapping Executable Images into Target Embedded Systems.		6	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6508	VLSI TESTING	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To know the various types of faults and also to study about fault detection and dominance.
- To know the concepts of test generation for combinational and sequential circuits
- To understand the concepts of test generation method – DFT, BIST.
- To understand the fault diagnosis method.

Syllabus

Introduction to Testing, Fault Modelling, Fault equivalence &collapsing.Logic and Fault Simulation, Testability Measures.Combinational ATPG-Sequential ATPG. Memory Test, Delay test , IDDQ testing. Design for testability – BIST, Boundary Scan standard. Introduction to Fault Diagnosis and Self-checking design.

Course Outcome:

The student will be able to:

1. Explain the VLSI testing procedure.
2. Analyze VLSI circuit for testability.
3. Understand basic ATPG Algorithms used in VLSI Testing.
4. Explain the delay testing, IDDQ testing and Memory Testing
5. Design logic circuit easier for testing by inserting elementary testing Hardware.

Text Books:

1. Viswani D Agarwal and Michael L Bushnell, “Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits”, Springer, 2000.

References:

1. M. Abramovici, M A Breuer and A D Friedman, “Digital systems Testing and Testable Design”, IEEE Press, 1994.
2. P.K. Lala, “Fault Tolerant and Fault Testable Hardware Design”, Academic Press, 2012.
3. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002
4. Alfred L Cronch, “Design for Test for Digital IC’s and Embedded Core system”, Prentice Hall, 1999.
5. NirajJha and Sanjeep K Gupta, “Testing of Digital Systems”, Cambridge University Press, 2003.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6508	VLSI TESTING	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction-Role of Testing -Yield-ATE Block Diagram.FaultModeling - glossary of Fault models - single stuck-at-faults-functional equivalence and fault collapsing Dominance collapsing and check point theorem.		6	15
MODULE 2: Logic and Fault Simulation -modeling signal states-algorithm for true value simulation-serial and parallel fault simulation Testability Measures-Combinational Controllability - Combinational Observability – Introduction to Sequential Testability Measures		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Combinational ATPG-Boolean Difference Method-D-Algorithm-PODEM-Sequential ATPG Implementation and complexity- Time Frame Expansion - simulation based methods.		7	15
MODULE 4: Delay test - Path delay test and fault models - Transition faults - delay test methodologies – practical consideration IDDQ testing – Faults detected by IDDQ Testing-Testing methods.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Memory Test-Faults & Fault modeling-March Test Algorithm-Reduced Functional Faults. Design for Testability – DFT Fundamentals, Scan design, Partial Scan, Random Access Scan,		8	20
MODULE 6: BIST- Pattern Generation-Output Response Analysis-BILBO. Boundary Scan standard.Introduction to Fault Diagnosis and Self-checking design.		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6512	INTRODUCTION TO MEMS	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To introduce the concepts of micro electromechanical devices.
- To understand the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators

Syllabus

MEMS Fundamental concepts ;Microfabrication techniques ; Photolithography, Ion Implantation, Diffusion, Oxidation, Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; etching techniques, Microsystems packaging; MEMS Sensors; MEMS Actuators.

Course Outcome:

The student will be able to:

1. describe new applications and directions of MEMS
2. Critically analyze microsystems technology for technical feasibility as well as practicality
3. Describe the limitations and current challenges in microsystems technology

Text Books:

1. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997.
2. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001

References:

1. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.
2. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006,
3. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press,2002

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6512	INTRODUCTION TO MEMS	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Micro scale systems overview, Introduction to MEMS,Applications. Devices and Structures for MEMS. Materials for MEMS		6	15
MODULE 2: Bulk Micromachining, Surface Micro machining High Aspect-Ratio (LIGA and LIGA-like) Technology		5	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating		6	15
MODULE 4: Dry and wet etching, electrochemical etching, Microsystems packaging, Essential packaging technologies, Selection of packaging materials,HTCC and LTCC		5	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Mechanics behind MEMS sensors, Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors, Piezo-resistive pressure sensor,thermal sensors, Magnetic sensors,radiation sensors		10	20
MODULE 6: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces, Micromechanical Motors and pumps. Comb drive actuators		10	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6514	DSP BASED SYSTEM DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To understand the concepts of different processor architectures and different DSP processors
- To understand the architecture AVR Microcontroller

Syllabus

Need for Special Digital Signal Processors :différent processor architectures : Introduction to AVR Microcontroller : Interfacing :Introduction to TI DSP processor : TMS330C6000: Introduction to the C6713 DSK" Review of FIR filtering: Review of IIR filtering: Writing efficient code: Introduction to Sharc/ Tiger Sharc/ Blackfin series

Course Outcome:

The student will be able to:
1. Explain the different processor architectures.
2. Program the DSP Processor

Text Books:

1. Dananjay V. Gadre 'Programming and Customizing the AVR microcontroller', McGraw Hill 2001
2. NaimDahnoun Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, 1st Edition
3. R. Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, John Wiley and Sons, Inc., New York, 2004.

References:

1. R. Barnett , L. O' CULL and S. Cox " Embedded C Programming and Atmel AVR", Delmar Cengage Learning, India Edition , 2009.
2. Sen M. Kuo and Woon-SengGan.Digital Signal Processors: Architectures, Implementations, and Applications, Prentice Hall ,2004
3. David J Defatta J, Lucas Joseph G &Hodkiss William S ;Digital Signal Processing: A System Design Approach, 1st Edition; John Wiley
4. A.V. Oppenheim and R.W. Schafer, Discrete-Time Signal Processing, Second edition, Prentice-Hall,Upper Saddle River, NJ, 1989

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6514	DSP BASED SYSTEM DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Need for Special Digital Signal Processors, Processor trends: Von Newmann versus Harvard architecture, Architectures of superscalar and VLIW fixed and floating point processors, New Digital Signal Processing hardware trends, Selection of DS processors.		7	15
MODULE 2: Introduction to AVR Micro controllers- Architecture – memory organization – addressing modes, I/O Memory – EEPROM – I/O Ports, SRAM –Timer –UART		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: AVR- Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing, Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing Introduction to TI DSP Processor -TMS330C6000 series		6	15
MODULE 4: TMS330C6000 series CPU Architecture, CPU Data Paths and Control, Internal Data/Program Memory. On chip peripherals: Timers - Multi channel buffered serial ports Extended Direct Memory Access, Interrupts, and Pipelining		9	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Design aspects:Introduction to the C6713 DSK- Code Composer Studio IDE - Matlab and basic skills, Review of FIR filtering: FIR filter design techniques and tools, Review of IIR filtering: IIR filter design techniques and tools, Sampling, quantization and working with the AIC23 codec		6	20
MODULE 6: Writing efficient code: optimizing compiler - effect of data types and memory map. TMS320C6713 Assembly language Programming: Instructions Set and Addressing Modes – Linear Assembly. Introduction to Sharc/ Tiger Sharc/ Blackfin series, Other major vendors in the DSP market and the latest trends.		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6516	HARDWARE AND SOFTWARE CODESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To educate the hardware, software, and system designer on the fundamentals of hardware/software co-design
- To understand and employ cooperative hardware/software design techniques for the construction of complex systems, particularly embedded systems.

Syllabus

Introduction: Motivation hardware & software co-design; Hardware Software back ground; Co-design Concepts; Methodology for Co-Design; Unified Representation for Hardware & Software; An Abstract Hardware & Software Model; Performance Evaluation; Object Oriented techniques in Hardware Design; Processor example.

Course Outcome:

The student will be able to employ cooperative hardware/software design techniques for the construction of complex systems, particularly embedded systems.

Text Books:

1. Sanjaya Kumar, James H.Ayler, "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002.
2. H.Kopetz, "Real-Time Systems", Kluwer, 1997.
3. R. Gupta, "Co-synthesis of Hardware and Software for Embedded Systems", Kluwer 1995.

References:

1. S. Allworth, "Introduction to Real-time Software Design", Springer-Verlag, 1984.
2. C. M. Krishna, K.Shin, "Real-time Systems", Mc-Graw Hill, 1997
3. Peter Marwedel, G. Goosens, "Code Generation for Embedded Processors", Kluwer Academic Publishers, 1995.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6516	HARDWARE AND SOFTWARE CODESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Specification of embedded systems- Why Co-design? – Comparison of co-design approaches-MoCs: State oriented, Activity oriented, Structure oriented, Data oriented and Heterogeneous- Software CFSMs-Processor Characterization.		7	15
MODULE 2: Introduction: Motivation hardware & software co-design, system design consideration, research scope &overviews. Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance modelling, Hardware Software development.		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Co-design Concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade-offs, co-design.		7	15
MODULE 4: Methodology for Co-Design: Amount of unification, general consideration & basic Philosophies, a framework for co-design Unified Representation for Hardware & Software: Benefits of unified representation, modelling concepts.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: An Abstract Hardware & Software Model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model. Performance Evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation		7	20
MODULE 6: Object Oriented techniques in Hardware Design: Motivation for object oriented technique, data types. Modelling hardware components as classes, designing specialized components, data decomposition, Processor example		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6518	VLSI DIGITAL SIGNAL PROCESSING	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
- Design and optimize VLSI architectures for basic DSP algorithms.
- Introduce algorithm, architecture, and circuit design tradeoffs to jointly optimize for power, performance, and area.

Syllabus

DSP algorithms. : Pipelining and Parallel Processing: Unfolding: Systolic architecture design : Arithmetic architecture: The CORDIC Algorithms : Fast convolution algorithms: Parallel FIR filters : Parallel processing in IIR filters.

Course Outcome:

The student will analyse and design basic signal processing blocks meeting VLSI constraints

Text Books:

1. Keshab V Parhi, VLSI Digital Signal Processing, Willey India.
2. Peter Pirsch, Architecture for Digital Signal Processing, Wiley

References:

1. Magdy A Bayoumi, VLSI design methodologies for DSP architecture.
2. B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford University Press, New York, 2010.
3. Israel Koren, Computer Arithmetic Algorithms, 2nd Edition, CRC Press, 2001
4. M.D. Ercegovac and T. Lang, Digital Arithmetic, Morgan Kaufmann Publishers - An Imprint of Elsevier Science, 2004

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6518	VLSI DIGITAL SIGNAL PROCESSING	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Representation of DSP algorithms. Iteration Bound: Loop Bound, Iteration Bound, LPM Algorithm for iteration bound computation, Iteration Bound for multirate data flow graphs		8	15
MODULE 2: Pipelining and Parallel Processing: Introduction,TimingTechniques:Retiming: introduction, properties, system inequalities, retiming techniques		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Unfolding: Introduction, algorithm, properties, critical pathSystolic architecture design: Introduction, Design Methodologies, Design B1 and B2		7	15
MODULE 4: Arithmetic architecture: Bit level arithmetic architecture, parallel multipliers, bit serial multipliers, Canonic Singed digit arithmetic, distributed arithmetic		6	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: The CORDIC Algorithms: Rotations and pseudo rotations, Basic CORDIC iterations, CORDIC hardware, Generalized CORDIC, Fast convolution algorithms: Cook Toom, Modified Cook-Toom		8	20
MODULE 6: Parallel FIR filters: Fast FIR, Pipelining of recursive filters:Introduction, pipeline interleaving, Parallel processing in IIR filters, Scaling and round off noise computation		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6522	RECONFIGURABLE COMPUTING	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To have fundamental knowledge and understanding of principles and practice in reconfigurable architecture and computing
- To study about Placement and partitioning algorithms.
- To familiarize various methods of reconfiguration
- To study reconfigurable architectures.

Syllabus

Introduction Reconfigurable Computing –- Performance, power, and other metrics - - RC Architectures - – Comparing Computing Machines. Placement and partitioning algorithms – Routing algorithms - Spatial Computing architectures – Systolic Architectures and Algorithms Systolic Structures –Adaptive Network Architectures – Reconfigurable bus – Dynamic reconfiguration– Partial reconfiguration – OS support – Reconfigurable Computing Architectures – Reconfigurable coprocessor based architectures – Reconfigurable pipelines – Reconfigurable memories & caches – Reconfigurable Computing Applications**.**

Course Outcome:

The student will be able to:

1. An ability to explain the reconfigurable computing architecture
2. An ability to use various algorithms for placement , partitioning and routing.
3. An ability to understand basic adaptive network architectures.

Text Books:

1. Wayne Wolf, “FPGA- based System Design”, Prentice Hall, 2004.

References:

1. R.Vaidynathan and J. I., Trahan, “Dynamic Reconfiguration: Architectures and Algorithms”, Khuwer Academic/Plenum Publishers, New York, 2004.
2. M. Gokhale and P. Graham, *Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays*, Springer, 2005, ISBN: 978-0-387-26105-8.
3. P. Lysaght and W. Rosenstiel (eds.), *New Algorithms, Architectures and Applications for Reconfigurable Computing*, Springer, 2005, ISBN: 978-1402031274.
4. D. Pellerin and S. Thibault, *Practical FPGA Programming in C*, Prentice-Hall, 2005, ISBN: 978-0131543188.
5. R. Cofer and B. Harding, *Rapid System Prototyping with FPGAs: Accelerating the Design Process*, Newnes, 2005, ISBN: 978-0750678667.
6. C. Bobda, *Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications*, Springer, 2007, ISBN: 978-1402060885.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6522	RECONFIGURABLE COMPUTING	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction to Adaptive/Reconfigurable Computing – Goals and motivations - History, state of the art, future trends, Basic concepts and related fields of study - Performance, power, and other metrics-Algorithm analysis and speedup projections, RC Architectures - Device characteristics - Fine-grained architectures - Coarse-grained architectures .– Custom Computing Machine Overview – Comparing Computing Machines		7	15
MODULE 2: Placement and partitioning algorithms, routing algorithms		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Spatial Computing architectures – Systolic Architectures and Algorithms Systolic Structures – Bit Serial. Reconfigurable coprocessor based architectures – Compiler technology for coprocessor based architectures.		6	15
MODULE 4: Adaptive Network Architectures – Static and Dynamic network – Routing/embedding Rearrange able networks. Reconfigurable bus – Dynamic reconfiguration issues – Reconfiguration delay – Partial reconfiguration – OS support.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Reconfigurable Operating Systems – Device and task models, Multitasking and runtime systems – Dynamically Reconfigurable Adaptive Viterbi Decoder		8	20
MODULE 6: Mapping/scheduling algorithm – Reconfigurable pipelines – Reconfigurable memories & caches. Reconfigurable Computing Applications**,** reconfigurability using Virtex T series		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6524	EMBEDDED CONTROL SYSTEM	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To introduce the concepts of embedded control systems.
- To understand various input out devices and data convertors
- To know the design concepts of asynchronous data communication as applied to ECS.

Syllabus

Basic concepts of Embedded Control System, schematic study ; Input and Output:Key board and displays; Timer and Interrupts; Serial Communication requirements; DAC and ADC, Ports, Data acquisition; Examples of Embedded Control System and case study.

Course Outcome:

The student will be able to:

1. Design interfacing circuits for embedded control system
2. Design and implement basic embedded control systems

Text Books:

1. Ball S.R,Embedded microprocessor Systems – Real World Design,Prentice Hall,2001

References:

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C”, The publisher, Paul Temme, 2003.
2. Herma K, “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 2003
3. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet”, PHI, 2002

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6524	EMBEDDED CONTROL SYSTEM	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Controlling the hardware with software, Data lines, Address lines, Ports – Schematic representation, Bit masking – Programmable peripheral interface		6	15
MODULE 2: Keyboard basics – Keyboard scanning algorithm., Switch input detection – 74 LS 244, Multiplexed LED displays Character LCD modules, LCD module display, Configuration		5	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Time-of-day clock –Timer manager, Interrupts – Interrupt service routines, IRQ, ISR, Interrupt vector or dispatch table multiple-point, Interrupt-driven pulse width modulation		6	15
MODULE 4: Asynchronous serial communication – RS-232, RS-485– Sending and receiving data, Serial ports on PC – Low-level PC serial I/O module, Buffered serial I/O.		5	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: DAC and ADC: R 2R ladder – Resistor network analysis, Port offsets – Triangle waves analog vs. digital values – ADC0809, Auto port detect – Recording and playing back voice, Capturing analog information in the timer interrupt service routine, Automatic, multiple channel analog to digital data acquisition.		10	20
MODULE 6: Multiple closure problems – Basic outputs with PPI, Controlling motors – Bi-directional control of motors, H bridge – Telephonic systems-Mobile and Satellite, Stepper control –Power electronic control systems		10	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6526	ELECTRONIC PACKAGING	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To understand the different electronic IC assembly and electrical design.
- To Understand the thermo mechanical design and materials used for electronic device packaging

Syllabus

Microsystems Packaging : Electrical Package Design: IC Assembly – Purpose, Requirements, Technologies, Printed Circuit Board – Anatomy, CAD tools for PCB design, Thermal Management : Design for Reliability – Fundamentals.

Course Outcome:

The student will be able to:

1. Get a detailed understanding of electronic Packaging Materials
2. Get a thorough idea about different IC Packaging
3. Get an idea about different thermal and electronic packaging considerations.

Text Books:

1. Rao R. Tummala: Fundamentals of Microsystem Packaging McGraw Hill.

References:

1. Richard K. Ulrich &William D. Brown Advanced Electronic Packaging - 2nd Edition : IEEE Press
2. Charles A Harper, Electronic Packaging and Interconnection Handbook, McGraw hill, Fourth Edition

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 6526	ELECTRONIC PACKAGING	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Microsystems Packaging- Need of packaging, electrical, mechanical and material technologies, Packaging Materials – electrical, thermal, mechanical and chemical properties. Future trends.		5	15
MODULE 2: Electrical Package Design: Fundamentals, Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip. Wafer Level Packaging – merits and demerits, Technologies, reliability, wafer level test.		8	15
MODULE 4: Printed Circuit Board – Anatomy, CAD tools for PCB design, Standard fabrication, Limitations, Microvia Boards. Board Assembly – Surface Mount Technology, Through-Hole Technology, Assembly Issues, Design challenges.		8	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Thermal Management - Cooling Requirements, Electronic cooling methods, Sealing and Encapsulation: Necessity, Requirements, Encapsulation Processes, Hermetic Sealing.		7	20
MODULE 6: Design for Reliability – Fundamentals, Induced failures, Design for Reliability – Fundamentals, Induced failures Electrical Testing – System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6592	MINI PROJECT	0-0-4:2	2015

COURSE CONTENT

The mini project is designed to develop practical ability and knowledge about practical tools/techniques in order to solve the actual problems related to the industry, academic institutions or similar area. Students can take up any application level/system level project pertaining to a relevant domain. At the end, presentation and demonstration of the project should be conducted, which will be evaluated by a panel of examiners.

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 6594	DESIGN LAB-II	0-0-2:1	2015

Course Objective:

To experiment the concepts introduced in the core and elective courses offered in the second semester with the help of simulation tools and related hardware.

Course Outcome:

The student will be able to design &analyzeanalog and digital circuits in CMOS.

	COURSE CONTENT	HRS
	Tools: CADENCE/SYNOPSYS/MENTOR GRAPHICS or any other equivalent tools	
PART A (Analog VLSI Design)	**Experiments:** Schematic Design, Simulation and Characterization of the following Analog Circuits a. OPAMP b. Two - Stage OPAMP with CMFB c. Comparator d. 8 - Bit Current Steering DAC/ Charge Scaling DAC e. 8- Bit SAR ADC	6
	MOSFET Device Characterization for Small Signal Device Parameters and Parasitics Design (Schematic and Layout), Simulation and Characterization of the following Analog Circuits a. Current Mirrors b. Voltage Reference c. Single Stage amplifier configurations i. CS ii. CG iii. CD d. Differential Amplifier	10
	Tools and Boards: XILINX/ALETERA or any other equivalent tools and Boards	

PART B (Embedded Experiments)	**I.** FPGA Based experiments (Simulation, Synthesis, Post Route Simulation) Digital Components inside a microprocessor and integration of these components a. Shifters b. State machine based controllers c. Instruction decoder d. ALU **II.** HDL Based experiments (All the experiments should be verified by downloading the programming file to FPGA/CPLD) a. Familiarization of User Constraints File and generation of programming file. b. IP Core based experiments c. Experiments on FPGA-on-board verification d. Implementation of digital filters (input may be taken using Parallel ADC and output may be observed using parallel DAC).	12

SEMESTER III

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7501	MIXED VLSI CIRCUITS DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To know the various types Mixed VLSI Circuit Design
- To know the concepts of switched capacitor filters and Applications
- To get a deep knowledge about ADC and DAC
- To know the working of analog and digital phase locked loops

Syllabus

Switched Capacitor Circuits, Switched Capacitor Integrators, z-Domain Models of Two-Phase Switched Capacitor Circuits D/A converter: ,Static non-idealities and Dynamic non-idealities, A/D Converter: Static non-idealities and Dynamic non-idealities, First and Second Order and Multi-bit Sigma-Delta Modulators, Basics of PLL, Basics of Delay Locked Loops

Course Outcome:

The student will be able to:

1. Explain Switched capacitor circuits.
2. Analyze the non-idealities of converter circuits and study various DAC circuits.
3. Understand various ADC circuits and modulator circuits.
4. Explain PLL, DLL and perform mixed-signal layout.
5. Explain Data transmission using current and voltage signalling.

Text Books:

1. BehzadRazavi, " Design of Analog CMOS Integrated Circuits", Tata Mc-Graw Hill.
2. CMOS mixed-signal circuit design by R. Jacob BakerWiley India, IEEE reprint 2008.
3. Paul R. Gray and Robert G.Meyer, " Analysis and Design of Analog Integrated Circuits", John Wiley & Sons.

References:

1. Alan B. Gnebene, " Bipolar and MOS analog integrated circuit design",John Wiley & Sons.
2. Mohammed I. Elmasy," Digital Bipolar circuits ", John Wiley & Sons.
3. Greogorian& Tames, "Analog Integrated Circuit For Switched Capacitor Circuit " , Wiley.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7501	MIXED VLSI CIRCUITS DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Continuous-Time Signal Processing-Sampled-Data Signal Processing. Switched Capacitor Circuits - Switched Capacitor Amplifiers- Switched Capacitor Integrators		6	15
MODULE 2: z-Domain Models of Two-Phase Switched Capacitor Circuits-First-Order Switched Capacitor Circuits Second-Order Switched Capacitor Circuits- Switched Capacitor Filters		5	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: D/A converter-General considerations. Static non-idealities and Dynamic non-idealities, Current – steering DAC-Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches		7	15
MODULE 4: A/D Converter- General considerations. Static non-idealities and Dynamic non-idealities. Flash ADC-Basic architectures. Successive Approximation ADC. Dual Slope A/D Converters -Pipe Line ADC. Hybrid ADC structures. Nyquist rate A/D Converters- Modulators for over sampled A/D Conversion		9	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: First and Second Order and Multi-bit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters. Basics of PLL. Analog PLL and Digital PLL Circuits		7	20
MODULE 6: Basics of Delay Locked Loops. Mixed-signal layout, Interconnects and data transmission. Data transmission using voltage mode signalling and current mode signalling.		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7503	SYSTEM ON CHIP	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- Provide an understanding of the concepts, issues, and process of System-on-Chip(SoC) design
- Understand hardware, software, and interface synthesis
- Analyze hardware/software tradeoffs
- Analyze the functional and non-functional performance of the system

Syllabus

Introduction to SoC Design, Platform based SoC design, MPSoC, Designing of Energy Aware MPSoC's, Introduction to MPSoC performance modelling, ASIC to System and NoC, Network topology,

Course Outcome:

The student will be able to understand the basic concepts of System on Chip

Text Books:

1. SudeepPasricha, NikilDutt ," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann, Elsevier, 2008

References:

1. Hoi-Jun Yoo, KangminLeeand Jun Kyong Kim, "Low Power NoC for High Performance SoC Design", CRC Press, 2008
2. Ahmed Amine Jerraya, Wayne Wolf, "Multiprocessor Systems-on-chips" , Morgan Kaufmann, Elsevier, 2005

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7503	SYSTEM ON CHIP	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Introduction to SoC Design, SoC Design Flow , Design Issues , Hardware software co-design		6	15
MODULE 2: Platform based SoC design, Basic concepts of bus based communication architectures, On chip communication architecture standards, MPSoC, Design challenges, Design Methodologies ,Hardware Architectures , Software		9	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Designing of Energy Aware MPSoC's: Processor Design, Memory System Design , On chip communication system design		6	15
MODULE 4: Introduction to MPSoC performance modeling , Architecture component performance modeling and analysis, Process execution modelling, Modeling shared resources, Global performance analysis		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: ASIC to System and NoC , Applications for MPSoC,, NoC for SoC design, Comparition of Bus based and NoC based SoC design		6	20
MODULE 6: Network topology , Switching Strategies , Routing algorithms , Flow control, Clocking schemes , Quality of Service (QoC) , NoC Architectures		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7505	COMPUTER ARCHITECTURE &PARALLEL PROCESSING	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

To understand computer architecture concepts and mechanisms related to the design of modern Processors & memories.

Syllabus

Fundamentals of Computer Design; Performance Measures. Instruction set architecture; Pipelined processors; resolving structural, data and control hazards; Memory Technology and Optimizations ; Memory Protection and Virtual Memory; Design of Memory Hierarchies; Analyzing memory performance; Models of Memory Consistency - Interconnection networks; Software and hardware multithreading -Design issues ;Case studies – Intel Multi-core architecture.

Course Outcome:

The student will be able to:

1. Know about the design of modern Processors & memories.
2. Analyse performance of processors.
3. Analyse various issues related to cache memories.

Text Books:

1. John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”,Morgan Kaufmann / Elsevier, 4th. edition, 2007

2. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.

References:

1. William Stallings, “Computer Organization and Architecture – Designing for Performance”,Pearson Education, Seventh Edition, 2006.
2. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
3. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997.
4. DimitriosSoudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012
5. John P. Shen, “Modern processor design. Fundamentals of super scalar processors”, TataMcGraw Hill 2003.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7505	COMPUTER ARCHITECTURE &PARALLEL PROCESSING	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors. Multivector and SIMD architectures – Multithreaded architectures – Data-flow architectures		6	15
MODULE 2: Performance Measures. Instruction set architecture; single - cycle processors; hardwired vs. microcoded FSM processors. Pipelined processors; resolving structural, data and control hazards.		8	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Analyzing processor performance - superscalar execution, out-of-order execution, register renaming, and memory disambiguation. Branch prediction, speculative execution; multithreaded, VLIW, and SIMD processors		7	15
MODULE 4: Memory Technology and Optimizations – Cache memory – direct-mapped vs. associative caches- write-through vs write-back caches. single-cycle, FSM, pipelined caches; Optimizations of Cache Performance – Memory Protection and Virtual Memory.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Design of Memory Hierarchies. Analyzing memory performance, Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues .		7	20
MODULE 6: Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches. Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7507	ELECTRONIC SYSTEM DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

To understand how an electronic system can design with least electromagnetic interference issues.

Syllabus

Product Design and Development: Product enclosure Design; Embedded System Development Environment: Electromagnetic Compatibility (EMC): Cabling of Electronic Systems: Grounding and Shielding: Electrostatic Discharge (ESD): System Design for EMC –PCB layout and stack up-

Course Outcome:

The student will be able to design an Embedded system which should have the least electromagnetic interference issues.

Text Books:

1. Shibu K.V , “Introduction to Embedded Systems”, Tata McGraw Hill, 2009
2. HenryW.Ott, “Electromagnetic Compatibility Engineering”, Wiley Interscience,2009

References:

1. Henry W.Ott, “Noise Reduction Techniques in Electronic Systems”, 2/e, WileyInterscience.
2. Clayton R.Paul , “Introduction to Electromagnetic Compatibility”, 2/e
3. Sonia Ben Dhia, Mohamed Ramdani, Etienne Sicard, “Electromagnetic Compatibility of Integrated Circuits Techniques for low emission and susceptibility”, Springer, 2006
4. David Morgan, “A Handbook for EMC Testing and Measurement”, 1/e, IET Electrical Measurement Series 8

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7507	ELECTRONIC SYSTEM DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Product Design and Development: Embedded System product Development Life cycle (EDLC), Objectives of EDLC, Phases of EDLC, modeling the EDLC, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development. Power supply Design.		7	15
MODULE 2: Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT). Electromagnetic Compatibility (EMC): Designing for EMC, EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic system.		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Cabling of Electronic Systems-Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling,, Magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, Inductive coupling-shielding properties of various cable configurations, coaxial cable versus shielded twisted pair, braided shields, ribbon cables.		7	15
MODULE 4: Grounding and Shielding: Safety grounds, signal grounds, single-point and multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, Common Mode Choke - shield grounding at high frequencies, guarded instruments.		6	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Common Mode Choke - shield grounding at high frequencies, guarded instruments. Near fields and far fields, characteristic and wave impedances, shielding effectiveness, absorption and reflection loss shielding with magnetic material, apertures, conductive gaskets, conductive windows, conductive coating, grounding of shields		7	20

MODULE 6: Electrostatic Discharge (ESD) - Static generation, human body model, static discharge, ESD protection in equipment design, Transient and Surge Protection Devices, software and ESD protection, ESD versus EMC, ESD Testing, System Design for EMC –PCB layout and stack up- General Printed Circuit Board Design considerations –PCB chassis and Ground connection, Return Path Discontinuities- PCB layer Stack up	8	20
END SEMESTER EXAM		

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7509	HIGH SPEED DIGITAL DESIGN	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To develop the skills for analyzing high-speed circuits with signal behaviour modelling
- To demonstrate proficiency in understanding signal integrity concepts and terminology and to understand the signal integrity on circuit design
- To be able to perform and analyze signal measurements and to be able to make trade off decisions based on signal budget and design requirements.

Syllabus

High Speed Digital Design Fundamentals; High Speed properties of Logic gates; Packaging of Digital Systems; Measurement Techniques; Transmission Lines; Problems of point to point wiring, signal distortion, EMI, cross talk; Ideal distortion less lossless transmission line; Transmission Lines at High frequency; Losses in transmission line- Skin effect, mechanics of skin effect, Proximity effect, Dielectric loss; Termination;. Vias; Connectors; Power system; Clock Distribution

Course Outcome:

The student will be able to:

1. Analyze the signal behaviour of high speed digital circuits.
2. Understand the signal integrity on circuit design.
3. Perform and analyze signal measurements.

Text Books:

1. Howard Johnson, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall
2. Dally W.S. &Poulton J.W., “Digital Systems Engineering”, Cambridge University Press.

References:

1. Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company

2. Jan M, Rabaey, Digital Integrated Circuits: A Design perspective, Second Edition, 2003.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7509	HIGH SPEED DIGITAL DESIGN	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: High Speed Digital Design Fundamentals: Frequency and time, Time and distance, lumped vs distributed Four kinds of reactance-ordinary capacitance and inductance, mutual capacitance and inductance, Relation of mutual capacitance and mutual inductance to cross talk. High Speed properties of Logic gates: Power, Quiescent vs active dissipation, Active power driving a capacitive load, Input power, Internal dissipation, drive circuit dissipation, Totem pole and open circuit speed, Sudden changes in voltage and current		8	15
MODULE 2: Packaging of Digital Systems: Integrated circuit packages, Wire and cable, Connectors .Measurement Techniques; Rise time and bandwidth of oscilloscope probes. Self inductance of probe ground loop, Effects of probe load on a circuit,		6	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Slow down of a system clock, observing cross talk, measuring operating margin, observing meta stable states. Transmission Lines; Problems of point to point wiring, signal distortion, EMI, cross talk,		7	15
MODULE 4: Ideal distortion less lossless transmission line, Transmission Lines at High frequency: Infinite uniform transmission line, Lossy transmission line, Low loss transmission line, RC transmission line, Skin effect, mechanics of skin effect, Proximity effect, Dielectric loss.		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Termination: End termination, Rise time, DC biasing, power dissipation, Source termination, Resistance value, Rise time, Power dissipation, Drive current, Middle terminators. Vias- mechanical properties, series inductance and capacitance of vias, Connectors – mutual, series and parasitic capacitance.		7	20
MODULE 6: Power system: Stable voltage reference, Uniform voltage distribution, resistance and inductance distribution wiring, series resistance and lead inductance of a capacitance Clock Distribution: schemes, Timing margin, Clock skew, delay		7	20

adjustments, Clock jitter		
END SEMESTER EXAM		

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7511	NANO DEVICES AND CIRCUITS	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To learn about leakage current and its control and reduction techniques in CMOS devices.
- To know the device technologies for sub 100nm CMOS.
- To study about various Nanoscale devices.
- To familiarize the low power design and voltage scaling issues in Nano scale devices.
- To design CMOS circuit using non-classical devices**.**

Syllabus

Leakage current mechanisms in nanoscale CMOS: Device technologies for sub 100nm CMOS: FINFETs: Surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs: Nanowire MOSFETs, Carbon nanotube MOSFETs: CMOS logic - power and performance: Sequential logic circuits,: CMOS circuit design using non-classical devices

Course Outcome:

The student will be able to:

1. Understand the basic concept of Nanoscale devices
2. Summarize the emerging Devices based on Nanotechnology.
3. Analyze various Nanoscale Circuits.
4. Interpret a simple low-power CMOS Nanoscale circuit

Text Books:

1. Lundstrom, M., “Nanoscale Transport: Device Physics, Modeling, and Simulation”, Springer. 2000

References:

1. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., “Strained-Si and Hetrostructure Field Effect Devices”, Taylor and Francis, 2007
2. Hanson, G.W., “Fundamentals of Nanoelectronics”, Pearson, India., 2008.
3. Wong, B.P., Mittal, A., Cao Y. and Starr, G., “Nano-CMOS Circuit and Physical Design”, Wiley, 2004

4. Lavagno, L., Scheffer, L. and Martin, G., “EDA for IC Implementation Circuit Design andProcess Technology”, Taylor and Francis, 2005

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7511	NANO DEVICES AND CIRCUITS	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, Process variations in devices and interconnects., Device technologies for sub 100nm CMOS: Silicidation and Cu-low k interconnects. Metal-high k gate. Emerging CMOS technologies at 32nm scale and beyond – FINFETs		7	15
MODULE 2: Surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs, Quantum confinement and tunneling in MOSFETs, Velocity saturation, carrier back scattering andinjection velocity effects. Si and hetero-structure		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Nanowire MOSFETs, Carbon nanotube MOSFETs, Quantum wells, quantum wires and quantum dots, Single electron transistors		6	15
MODULE 4: CMOS logic - power and performance, Voltage scaling issues, Introduction to low power design, Performance optimization for data paths		8	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Sequential logic circuits, Timing and clock distribution, I/O circuits and memory design and trends		7	20
MODULE 6: CMOS circuit design using non-classical devices –FINFETs, nanowire, CMOS circuit design using non-classical devices – carbon nanotubes and tunnel devices		7	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7513	POWER MANAGEMENT OF EMBEDDED SYSTEMS	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To develop a basic understanding of dc-dc converter circuits
- To gain familiarity in digital circuit power distribution

Syllabus

Non-isolated DC-DC converters: buck converter: boost converter: buck-boost converter: Selection of power devices, Isolated converters: Pulse Width Modulation-: PWM through Phase Modulation: Digital circuit power distribution: decoupling capacitors: embedded PCB capacitance.

Course Outcome:

The student will be able to understand the basic concept of Power Supply Converters and power management methods for Embedded Systems.

Text Books:

1. L. Umanand, “Power electronics essentials and applications”, Wiley India, 2009.

References:

1. Henry W. Ott, “Electromagnetic Compatibility Engineering”, John Wiley & Sons, 2009.
2. Clayton R. Paul, “Introduction to Electromagnetic Compatibility”, John Wiley & Sons, 2006.
3. Mark I. Montrose, “EMC and the printed circuit board”, John Wiley & Sons, 1998.
4. Howard W. Johnson and Martin Graham, “High speed digital design”, Prentice Hall, 1993.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7513	POWER MANAGEMENT OF EMBEDDED SYSTEMS	3-0-0:3	
MODULES		Contact Hours	Sem. Exam Marks (%)
MODULE 1: Non-isolated DC-DC converters: Single pole double throw switch, chopper, DC steady state, buck converter, steady state analysis, effect of non-idealities, boost converter, steady state analysis, effect of non-idealities, buck-boost converter, steady state analysis, effect of non-idealities.		8	15
MODULE 2: Selection of power devices, continuous and discontinuous conduction modes, Isolated converters: forward converter, demagnetizing winding, dual switch forward converter, push-pull converter.		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Half-bridge converter, full-bridge converter, flyback converter, Cuk converter, soft switching in converters, zero-current and zero voltage switching.		6	15
MODULE 4: Inverter topologies, self driven inverters, Push -Pull configurations, half-bridge Configuration, Full-Bridge configuration, Three Phase inverter Topologies,		6	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Pulse Width Modulation- Quasi-Square Modulation, End pulse Modulation, Center Pulse Modulation, PWM through Phase Modulation, Sinusodial Pulse Width Modulation.		6	20
MODULE 6: Digital circuit power distribution: power supply decoupling, transient power supply currents, transient load current, Fourier spectrum, decoupling capacitors, effective decoupling strategies, multiple decoupling capacitors, target impedance, embedded PCB capacitance, power supply isolation, the effect of decoupling on radiated emissions, decoupling capacitor selection, placement and mounting.		9	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7515	VLSI FOR WIRELESS COMMUNICATION	3-0-0:3	2015

Pre-requisites: nil

Course Objectives:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To understand the concepts of CDMA in wireless communication

Syllabus

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Balancing Mixer: Switching Mixer: Sampling Mixer: Data converters in communications: Switch Capacitor Amplifiers: ADC: VLSI architecture for Multitier Wireless System

Course Outcome:

The student will be able to design a VLSI system for wireless communication

Text Books:

1. BehzadRazavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 1999.
2. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.

References:

1. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,1998.
2. Thomas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits’, Cambridge University Press ,2003.
3. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design - Circuits and Systems”, KluwerAcademic Publishers, 2000.
4. Andreas.F. Molisch, “Wireless Communications”, John Wiley – India, 2006.
5. VLSI Architectures for Multitier Wireless Systems by Joseph R. Cavallaro, 1999.
6. Equalization concept – a tutorial – application report by David Amalley, Atlanta Regional Technology Center.

COURSE PLAN

COURSE CODE:	COURSE TITLE	CREDITS	
04 EC 7515	VLSI FOR WIRELESS COMMUNICATION	3-0-0:3	
MODULES		**Contact Hours**	**Sem. Exam Marks (%)**
MODULE 1: Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier, Design - Wideband LNA - Design Narrowband LNA, Impedance Matching - Automatic Gain Control Amplifiers, Power Amplifiers		8	15
MODULE 2: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer.		7	15
INTERNAL TEST 1 (MODULE 1 & 2)			
MODULE 3: Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.		5	15
MODULE 4: Data converters in communications- Sampling Circuits (NMOS, PMOS and CMOS Switches), Distortion due to the Sampling Switch, Thermal Noise in Sample and Holds, Charge Injection in a Sampling Switch. Bottom Plate Sampling, The Gate Bootstrapped Switch. Characterizing a Sample-and-Hold, FFT Leakage and the Rectangular Window. Spectral Windows, the Hann Window		7	15
INTERNAL TEST 2 (MODULE 3 & 4)			
MODULE 5: Switch Capacitor Amplifiers- Parasitic Insensitive SC Amplifiers, Fully Differential SC-circuits, ADC- ADC Terminology, Offset and Gain Error, Differential Nonlinearity (DNL). Integral Nonlinearity (INL), Flash A/D Converter, oversampling converter. D/A Converter- INL/DNL, DAC Spectra and Pulse Shapes, Current Steering DAC-Current Cell Design.		7	20
MODULE 6: VLSI architecture for Multitier Wireless System, Equalizers– Inter Symbol interference, pulse shaping, Equalization – multi path effect on frequency response, zero forcing equalization, Hardware Design Issues for a Next generation CDMA Systems		8	20
END SEMESTER EXAM			

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7591	SEMINAR II	0-0-2:2	2015

COURSE CONTENT

Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the third semester of the M. Tech. Programme. He / she shall select the topic based on the References: from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7593	PROJECT (PHASE 1)	0-0-12:6	2015

COURSE CONTENT

In Project Phase-I, the students should select an emerging research area in the field that has direct or indirect relation to the area of specialization. After conducting a detailed literature survey, they should compare and analyze research work done and review recent developments in the area and prepare an initial design of the work to be carried out. It is mandatory that the students should refer National and International Journals and conference proceedings while selecting a topic for their project. He/She should select a recent topic from a reputed International Journal, preferably IEEE, ACM, Springer. Emphasis should be given for introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work carried out on the project topic.

Students should submit a copy of Phase-I project report covering the content discussed above and highlighting the features of work to be carried out in Phase-II of the project. The candidate should present the current status of the project work and the assessment will be made on the basis of the work and the presentation, by a panel of internal examiners in which one will be the internal guide. The examiners should give their suggestions in writing to the students so that it should be incorporated in the Phase–II of the project.

SEMESTER IV

COURSE CODE	COURSE NAME	L-T-P:C	YEAR
04 EC 7594	PROJECT (PHASE 2)	0-0-21:12	2015

COURSE CONTENT

In the fourth semester, the student has to continue the project phase-I work and after successfully finishing the work, he / she has to submit a detailed bounded project report. The work carried out should lead to a publication in a National / International Conference or Journal. The papers received acceptance before the M.Tech evaluation will carry specific weightage.