ST. JOSEPH'S
COLLEGE OF ENGINEERING
AND TECHNOLOGY,
- PALAI -
AUTONOMOUS

SJCET M.Tech (VLSI & ES) Curriculum 2024

(M.Tech in VLSI and Embedded Systems)

Signed By:Devassia V P
Approved by SJCET Academic Council held on 29.11.2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech- VLSI & Embedded Systems

SEMESTER I

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
A	24SJ1TEC100	ADVANCED ENGINEERING MATHEMATICS	40	60	3-0-0	3	3
B	24SJ1TEC006	CMOS VLSI DESIGN	40	60	3-0-0	3	3
C	24SJ1TEC007	FPGA BASED SYSTEM DESIGN	40	60	3-0-0	3	3
D	24SJ1EECXXX	PROGRAM ELECTIVE 1	40	60	3-0-0	3	3
E	24SJ1EECXXX	PROGRAM ELECTIVE 2	40	60	3-0-0	3	3
S	24SJ1RGE100	RESEARCH METHODOLOGY AND IPR	40	60	2-0-0	2	2
T	24SJ1LEC003	DESIGN LAB I	100	--	0-0-2	2	1
Total			**340**	**360**		**19**	**18**

Teaching Assistance: 6 hours

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M. Tech- VLSI & Embedded Systems

PROGRAM ELECTIVE 1

PROGRAM ELECTIVE 1						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
D	1	24SJ1EEC034	PHYSICAL DESIGN AUTOMATION	3-0-0	3	3
	2	24SJ1EEC035	DESIGN WITH ADVANCED MICROCONTROLLER	3-0-0	3	3
	3	24SJ1EEC036	EDA TOOLS	3-0-0	3	3
	4	24SJ1EEC037	DSP ALGORITHMS AND ARCHITECTURE	3-0-0	3	3
	5	24SJ1EEC038	ADVANCED DIGITAL SIGNAL PROCESSING	3-0-0	3	3
	6	24SJ1EEC007	ELECTRONIC PACKAGING	3-0-0	3	3

PROGRAM ELECTIVE 2

PROGRAM ELECTIVE 2						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
E	1	24SJ1EEC039	VLSI SIGNAL PROCESSING	3-0-0	3	3
	2	24SJ1EEC101	ADVANCED DIGITAL SYSTEM DESIGN	3-0-0	3	3
	3	24SJ1EEC040	DIGITAL DESIGN PRINCIPLES AND APPLICATIONS	3-0-0	3	3
	4	24SJ1EEC041	FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG	3-0-0	3	3
	5	24SJ1EEC042	ASIC DESIGN	3-0-0	3	3
	6	24SJ1EEC043	EMBEDDED OPERATING SYSTEM	3-0-0	3	3
	7	24SJ1EEC011	REAL TIME OPERATING SYSTEM	3-0-0	3	3

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SEMESTER II

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
A	24SJ2TEC100	FOUNDATIONS OF DATA SCIENCE	40	60	3-0-0	3	3
B	24SJ2TEC004	ANALOG VLSI DESIGN	40	60	3-0-0	3	3
C	24SJ2EECXXX	PROGRAM ELECTIVE 3	40	60	3-0-0	3	3
D	24SJ2EECXXX	PROGRAM ELECTIVE 4	40	60	3-0-0	3	3
E	24SJ2EECXXX	INDUSTRY/ INTERDISCIPLINARY ELECTIVE	40	60	3-0-0	3	3
S	24SJ2PEC100	MINI PROJECT	100	--	0-0-4	4	2
T	24SJ2LEC003	DESIGN LAB II	100	--	0-0-2	2	1
Total			**400**	**300**		**21**	**18**

Teaching Assistance: 6 hours

PROGRAM ELECTIVE 3

PROGRAM ELECTIVE 3						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
C	1	24SJ2EEC035	EMBEDDED NETWORKING	3-0-0	3	3
	2	24SJ2EEC043	SoC DESIGN	3-0-0	3	3
	3	24SJ2EEC036	VLSI STRUCTURE FOR DSP	3-0-0	3	3
	4	24SJ2EEC037	SEMICONDUCTOR MEMORIES	3-0-0	3	3
	5	24SJ2EEC038	EMBEDDED SYSTEM DESIGN	3-0-0	3	3
	6	24SJ2EEC039	MULTIRATE SIGNAL PROCESSING AND WAVELETS	3-0-0	3	3

PROGRAM ELECTIVE 4

PROGRAM ELECTIVE 4						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
D	1	24SJ2EEC040	LOW POWER VLSI	3-0-0	3	3
	2	24SJ2EEC041	VLSI SYSTEM TESTING	3-0-0	3	3
	3	24SJ2EEC042	HIGH SPEED DIGITAL DESIGN	3-0-0	3	3
	4	24SJ2EEC021	DEEP LEARNING	3-0-0	3	3
	5	24SJ2EEC044	STATIC TIMING ANALYSIS	3-0-0	3	3
	6	24SJ2EEC045	SIGNAL COMPRESSION	3-0-0	3	3

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INTERDISCIPLINARY ELECTIVE

INTERDISCIPLINARY ELECTIVE						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
E	1	24SJ2EEC083	AUTOMOTIVE ELECTRONICS	3-0-0	3	3
	2	24SJ2EEC084	MEMS AND SENSORS	3-0-0	3	3
	3	24SJ2EEC085	NANO MATERIALS FOR DRUG DELIVERY	3-0-0	3	3

INDUSTRY ELECTIVE

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SEMESTER III

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
TRACK 1							
A*	24SJ3MECXXX	MOOC	To be completed successfully		--	--	2
B	24SJ3AGEXXX	AUDIT COURSE	40	60	3-0-0	3	-
C	24SJ3IEC100	INTERNSHIP	50	50	--	--	3
D	24SJ3PEC100	DISSERTATION PHASE 1	100	--	0-0-17	17	11
TRACK 2							
A*	24SJ3MECXXX	MOOC	To be completed successfully		--	--	2
B	24SJ3AGEXXX	AUDIT COURSE	40	60	3-0-0	3	-
C	24SJ3IEC100	INTERNSHIP	50	50	---	--	3
D	24SJ3PEC001	RESEARCH PROJECT PHASE 1	100	--	0-0-17	17	11
Total			**190**	**110**		**20**	**16**

Teaching Assistance: 6 hours

*MOOC Course to be successfully completed before the commencement of fourth semester (starting from semester 1).

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AUDIT COURSE

AUDIT COURSE						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
B	1	24SJ3AGE100	ACADEMIC WRITING	3-0-0	3	-
	2	24SJ3AGE001	ADVANCED ENGINEERING MATERIALS	3-0-0	3	-
	3	24SJ3AGE002	FORENSIC ENGINEERING	3-0-0	3	-
	4	24SJ3AGE003	DATA SCIENCE FOR ENGINEERS	3-0-0	3	-
	5	24SJ3AGE004	DESIGN THINKING	3-0-0	3	-
	6	24SJ3AGE005	FUNCTIONAL PROGRAMMING IN HASKELL	3-0-0	3	-
	7	24SJ3AGE006	FRENCH LANGUAGE (A1 LEVEL)	3-0-0	3	-
	8	24SJ3AGE007	GERMAN LANGUAGE (A1 LEVEL)	3-0-0	3	-
	9	24SJ3AGE008	JAPANESE LANGUAGE (N5 LEVEL)	3-0-0	3	-
	10	24SJ3AGE009	PRINCIPLES OF AUTOMATION	3-0-0	3	-
	11	24SJ3AGE010	REUSE AND RECYCLE TECHNOLOGY	3-0-0	3	-
	12	24SJ3AGE011	SYSTEM MODELING	3-0-0	3	-
	13	24SJ3AGE012	EXPERT SYSTEMS	3-0-0	3	-

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SEMESTER IV

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
TRACK 1							
A	24SJ4PEC100	DISSERTATION PHASE II	100	100	0-0-24	24	16
TRACK 2							
A	24SJ4PEC001	RESEARCH PROJECT PHASE II	100	100	0-0-24	24	16
Total			**100**	**100**		**24**	**16**

Teaching Assistance: 5 hours

SYLLABUS

M. Tech.

ELECTRONCS AND COMMUNICATION ENGINEERING

(VLSI & EMBEDDED SYSTEMS)

2024 SCHEME

ST. JOSEPH'S
COLLEGE OF ENGINEERING AND TECHNOLOGY, - PALAI -
AUTONOMOUS

Vision

Developing into a world class, pace setting institute of Engineering and Technology with distinct identity and character, meeting the goals and aspirations of the society.

Mission

- To maintain a conducive infrastructure and learning environment for world class education.
- To nurture a team of dedicated, competent and research-oriented faculty.
- To develop students with moral and ethical values, for their successful careers, by offering variety of programs and services.

Department of

Electronics and Communication Engineering

Vision

Develop into a center of excellence in Electronics and Communication Engineering contributing to socio-economic progress.

Mission

- To develop and maintain adequate infrastructure for a pace-setting Electronics and Communication engineering.
- To bring up a team of committed, proficient and research-oriented electronics and communication engineering faculty.
- To nurture students into ethical, emotionally strong and technically competent graduates to meet the dynamic challenges of the society.

Programme Outcomes (POs)

PO1: An ability to independently carry out research/investigation and development work in engineering and allied streams

PO2: An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.

PO3: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program

PO4: An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards.

PO5: An ability to identify, select and apply appropriate techniques, resources and state- of-the-art tools to model, analyze and solve practical engineering problems.

PO6: An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects

PO7: An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Programme Specific Outcomes (PSOs)

Post Graduates of the program will be able to:

- Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and prototype development focusing on applications.
- Integrate multiple sub-systems to develop System On Chip, optimize its performance and excel in industry sectors related to VLSI/ Embedded domain.

SEMESTER I

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
A	24SJ1TEC100	ADVANCED ENGINEERING MATHEMATICS	40	60	3-0-0	3	3
B	24SJ1TEC006	CMOS VLSI DESIGN	40	60	3-0-0	3	3
C	24SJ1TEC007	FPGA BASED SYSTEM DESIGN	40	60	3-0-0	3	3
D	24SJ1EECXXX	PROGRAM ELECTIVE 1	40	60	3-0-0	3	3
E	24SJ1EECXXX	PROGRAM ELECTIVE 2	40	60	3-0-0	3	3
S	24SJ1RGE100	RESEARCH METHODOLOGY AND IPR	40	60	2-0-0	2	2
T	24SJ1LEC003	DESIGN LAB I	100	--	0-0-2	2	1
Total			**340**	**360**		**19**	**18**

Teaching Assistance: 6 hours

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1TEC100	ADVANCED ENGINEERING MATHEMATICS	DISCIPLINE CORE	3	0	0	3

Preamble: The purpose of this course is to expose students to the basic theory of linear algebra and probability.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	To analyze distributions of random variables and make computations based on that
CO 2	evaluate average behaviour of random variables, and analyze their converging behviours
CO 3	To analyze behaviour of random processes and explain basis of vector spaces.
CO 4	To evaluate properties of linear transformations
CO 5	To evaluate if a linear tranformaion is diagonalizable and decompose it using spectral decomposition theorem.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO4	PO5	PO6	PO7	PSO1	PSO2
CO 1	3		3		3	3			
CO 2	3		3		3	3			
CO 3	3		3		3	3			
CO 4	3		3		3	3			
CO 5	3		3		3	3			

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	20
Create	

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

Micro project/Course based project : 20marks
Course based task/Seminar/Quiz : 10marks
Test paper, 1 no. : 10 marks

The project shall be done individually. Group projects are not permitted. The project may include the implementation of theoretical computation using software packages.
The test papers hall includes a minimum 80% of the syllabus.

End Semester Examination Pattern:

End Semester Examination: 60 marks

There will be two parts; Part A and Part B

- Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions.
- Part B will contain 7 questions with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Syllabus

Module 1 Axiomatic definition of probability. Independence. Bayes' theorem and applications. Random variables. Cumulative distribution function, Probability Mass Function, Probability Density function, Conditional and Joint Distributions and densities, Independence of random variables. Functions of Random Variables: Two functions of two random variables. Pdf of functions of random variables using Jacobian.

Module 2 Expectation, Fundamental theorem of expectation, Moment generating functions, Characteristic function. Conditional expectation. Covariance matrix. Uncorrelated random variables. Pdf of Jointly Gaussian random variables, Markov and Chebyshev inequalities, Chernoff bound. Central Limit theorem. Convergence of random variables. Weak law of large numbers, Strong law of large numbers.

Module 3 Random Processes. Poisson Process, Wiener Process, Markov Process, Birth- Death Markov Chains, Chapman- Kolmogorov Equations,

Groups, Rings, homomorphism of rings. Field. Vector Space. Subspaces. direct sum. Linear independence, span. Basis. Dimension. Finite dimensional vector spaces. Coordinate representation of vectors. Row spaces and column spaces of matrices.

Module 4 Linear Transformations. Four fundamental subspaces of a linear transformation. Rank and Rank-nullity theorem. Matrix representation of linear transformation. Changeof basis transformation. System of linear equations. Existence and uniqueness of solutions. Linear functionals. Dual, double dual and transpose of a linear transformation.

Module 5 Eigen values, Eigen vectors, Diagonizability.

Inner product. Norm. Projection. Least-squares solution. Cauchy-Schwartz inequality. Orthonormal bases. Orthogonal complement. Spectral decomposition theorem.

M.TECH DEGREE EXAMINATION
SEMESTER:
ADVANCED ENGINEERING MATHEMATICS

Time: 2.5 Hours **Marks: 60**

Part A

Answer ALL Questions. Each question carries 5 marks

1. Given that $ff(x) = \frac{k}{2^x}$ is a probability distribution of a random variable that can take on the values $x = 0,1,2,3,A\ 4$. Find k. Find the cumulative distribution function.
2. State and prove weak law of large numbers.
3. Show that $(1,3,2,-2), (4,1,-1,3), (1,1,2,0), (0,0,0,1)$ is a basis for R^4.
4. Let $T: V \rightarrow W$be a linear transformation defined by $T(x,y,z) = (x+y, x-y, 2x+z)$. Find the range, null space, rank and nullity of T.
5. Describe an inner product space. If V is an inner product space, then for any vectors α, βin V prove that $\|\alpha+\beta\| \leq \|\alpha\| + \|\beta\|$.

Part B

Answer ANY FIVE Questions, one from each module
(5 x 7 marks = 35marks)

6. If the probability mass function of a RV X is given by $P(X = x) = kx^3, x = 1,2,3,4$. Find the value of k, $P(\frac{1}{2} < X < \frac{3}{2} / X > 1)$ mean and variance of X.
7. If the moment generating function of a uniform distribution for a random variable X is $\frac{1}{t}(e^{5t} - e^{4t})$.Find E(X).
8. Consider the Markov chain with three states, s={1,2,3} that has the following transition matrix $P = \begin{bmatrix} \frac{1}{2} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{3} & 0 & \frac{2}{3} \\ \frac{1}{2} & \frac{1}{2} & 0 \end{bmatrix}$ Draw the state diagram for the chain. If $P(X_1 = 1) = P(X_2 = 2) = \frac{1}{4}$, find $P(X_1 = 3, X_2 = 2, X_3 = 1)$.
9. Find the eigen values and eigen vectors of $A = \begin{bmatrix} 2 & 2 & 1 \\ 1 & 3 & 1 \\ 1 & 2 & 2 \end{bmatrix}$

10. Find the least square solution to the equation $Ax = b$, where $A = \begin{bmatrix} 1 & 2 \\ 1 & 3 \\ 0 & 0 \end{bmatrix}$ and $b = \begin{bmatrix} 4 \\ 5 \\ 6 \end{bmatrix}$. Obtain the projection matrix P which projects b on to the column space of A.
11. Let T be the linear transformation from R^3 to R^2 defined by T(x,y,z) =(x+y, 2z-x). Let B_1, B_2 be standard ordered bases of R^3 and R^2 respectively. Compute the matrix of T relative to the pair B_1, B_2.
12. Let V be a finite-dimensional complex inner product space, and let T be any linear operator on V. Show that there is an orthonormal basis for V in which the matrix of T is upper triangular.

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No	Topic	No. of Lectures
	Module I	
1.1	Axiomatic definition of probability. Independence. Bayes' theorem and applications.	2
1.2	Random variables. Cumulative distribution function, Probability Mass Function,	1
1.3	Probability Density function, Conditional and Joint Distributions and densities, Independence of random variables.	2
1.4	Functions of Random Variables: Two functions of two random variables. Pdf of functions of random variables using jacobian.	2
	Module II	
2.1	Expectation, Fundamental theorem of expectation, Conditional expectation.	1
2.2	Moment generating functions, Charectristic function.	1
2.3	Covariance matrix. Uncorrelated random variables. Pdf of Jointly Guassian random variables,	2
2.4	Markov and Chebyshev inequalities, Chernoff bound. Central Limit theorem.	2
2.5	Convergence of random variables. Weak law of large numbers, Strong law of large numbers.	2
3	**Module III**	
3.1	Random Processes. Poisson Process, Wiener Process,	2
3.2	Markov Process, Birth-Death Markov Chains, Chapman-Kolmogorov Equations,	2
3.3	Groups, Rings, homomorphism of rings. Field. Vector Space. Subspaces. direct sum.	2
3.4	Linear independence, span. Basis. Dimension. Finite dimensional vector spaces.	2
3.5	Coordinate representation of vectors. Rowspaces and column spaces of matrices.	1
4	**Module IV**	
4.1	Linear Transformations. Four fundamental subspaces of a linear transformation. Rank and Rank-nullity theorem.	2
4.2	Matrix representation of linear transformation. Change of basis transformation.	1
4.3	System of linear equations. Existence and uniqueness of solutions.	2
4.4	Linear functionals. Dual, double dual and transpose of a linear transformation.	2

5	**Module V**	
5.1	Eigen values, Eigen vectors, Diagonizability.	2
5.2	Inner product. Norm. Projection. Least-squares solution. Cauchy-Schwartz inequality.	2
5.3	Orthonormal bases. Orthogonal complement. Spectral decomposition theorem.	2

Reference Books

1. Hoffman Kenneth and Kunze Ray, Linear Algebra, Prentice Hall of India.

2. Jimmie Gilbert and Linda Gilbert, Linear Algebra and Matrix Theory, Elsevier

3. Henry Stark and John W. Woods "Probability and Random Processes withApplications to Signal Processing", Pearson Education, Third edition.

4. Athanasios Papoulis and S. Unnikrishna Pillai. Probability, Random Variables and Stochastic Processes, TMH

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1TEC006	CMOS VLSI DESIGN	PROGRAM CORE 1	3	0	0	3

Preamble: This course aims to develop students a good knowledge of all aspects of CMOS VLSI Design, its characteristics, designing and model various subsystems using CMOS logic.

Course Outcomes: After the completion of the course the student will be able to:

CO 1	Design Basic CMOS Digital Circuits.
CO 2	Demonstrate Delay Models, Interconnect, Power Analyses, I/O and Clocking Issues of CMOS Digital Circuits.
CO 3	Design Various Types of Static and Dynamic Digital CMOS Circuits.
CO 4	Demonstrate the Timing Concepts in Latch and Flip-Flops.
CO 5	Design CMOS Data Path Subsystems and Memory Arrays.

Mapping of Course Outcomes with Program Outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3	-	3	2	3	2	1	1	
CO 2	--	-	3	2	3	2	-	2	1
CO 3	3	-	3	2	3	2	1	2	
CO 4	-	-	3	2	3	2	-	2	2
CO 5	3	-	3	2	3	2	1	2	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30 %
Analyse	30 %
Evaluate	30 %
Create	10 %

Mark Distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks Test paper, 1 no. : 10 marks

The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

The end semester examination will be conducted by the institute. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 5 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 7 marks. Total duration of the Examination will be 150 minutes.

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS) FIRST SEMESTER M.TECH DEGREE EXAMINATION			Name Register No:
Course code	**24SJ1TEC006**	Course name	CMOS VLSI DESIGN
Max. Marks	60	Duration	2.5 Hours

PART A (Answer all questions. Each question carries 5 marks)
1. Illustrate different Types of Power Dissipation in CMOS.
2. Demonstrate the crosstalk effects in interconnect used in ICs. How can we eliminate crosstalk.
3. Illustrate the problem of monotonicity in dynamic CMOS circuits. How it can be eliminated.
4. Distinguish Max-Delay Constraints and Min-Delay Constraints.
5. Discuss Embedded DRAM.
PART B (Answer any 5 questions. Each question carries 7 marks)
6. Sketch the DC characteristics of CMOS inverter.
7. Design a 3 input AND gate with equal rise and fall resistance. Model the circuit using RC network. Find the worst-case Elmore parasitic delay of 3 input AND gate.
8. Consider a 3 mm-long, 100nm wide wire. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF/μm. Construct a π-model for the wire.
9. Design a 3-input BiCMOS NAND gate. Label the transistor widths. What is the logical effort.
10. Discuss the concept of TSPC based latches.
11. Illustrate the booth encoding techniques used in multipliers
12. Design 6T SRAM cell. How read and write operations are performed.

Module I (7 Hrs)

Introduction to CMOS technology: MOS Transistor operations (Enhancement and depletion type), Structured Design -Y Diagram.

Static CMOS Inverter: DC Characteristics, Beta Ratio Effects, Noise Margin- Basics, Pass Transistor DC Characteristics.

Power analysis: Types of Power Dissipation, On-Chip Power Distribution Network. On- Chip Bypass Capacitance, Power Network Modelling, Power Supply Filtering, Charge Pumps. Energy Scavenging.

Module II (10 Hrs)

Delay Models: Introduction, Definitions, Timing Optimization. RC Delay Model: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits, Elmore Delay, Layout Dependence of Capacitance, Determining Effective Resistance. Linear Delay Model: Logical Effort, Parasitic Delay, Delay in a Logic Gate. Logical Effort of Paths: Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Example.

Interconnect: Introduction, Wire Geometry, Interconnect Modelling: Resistance, Capacitance, Inductance (Pi modelling). Interconnect Impact: Delay, Energy, Crosstalk, Effective Resistance and Elmore Delay.

Clocks: Clock System Architecture, Global Clock Generation, Global Clock Distribution, Local Clock Gaters, Adaptive Deskewing, PLLs and DLLs.

I/O: Basic I/O Pad Circuits, Electrostatic Discharge Protection.

Module III (7 Hrs)

Combinational Circuit Design: Static CMOS circuits, Combinational logic circuits, Ratioed Circuits. **Dynamic logic:** Domino Logic, Dual-Rail Domino Logic, Keepers, Multiple-Output Domino Logic (MODL), NP Domino logic (NORA).

BiCMOS logic gates: Inverter, NAND, NOR. Introduction to **Silicon-On-Insulator Circuit Design**

Module IV (8 Hrs)

Sequential Circuit Design: Sequencing Static Circuits-Flip-flops and latches**.**
Sequencing Methods: Max-Delay Constraints, Min-Delay Constraints, Time Borrowing, Clock Skew. **Circuit Design of Latches and Flip-Flops:** Conventional CMOS Latches, Conventional CMOS Flip-Flops, True Single-Phase-Clock (TSPC) Latches and Flip-Flops.

Data path Subsystems:

Adders: Single-Bit Addition, Carry-Propagate Addition, Multiple-Input Addition
Multipliers: Unsigned Array Multiplication, Booth Encoding**.**
Shifters: Funnel Shifter, Barrel Shifter. **Comparators:** Magnitude Comparator.
Counters: Binary Counters.
Designing of memory and array structures: SRAM, DRAM, and Embedded DRAM.Read-Only Memory.

Course Plan

No	Topic	No. of Lectures
1	**Module I (7 Hrs)**	
1.1	**Introduction to CMOS technology**:	
	MOS Transistor operations (Enhancement and depletion type)	1
	Structured Design -Y Diagram	1
1.2	**Static CMOS Inverter**:	
	DC Characteristics	1
	Beta Ratio Effects, Noise Margin-Basics, Pass Transistor DC Characteristics	1
1.3	**Power analysis**:	
	Types of Power Dissipation	1
	On-Chip Power Distribution Network, On-Chip Bypass Capacitance	1
	Power Network Modelling, Power Supply Filtering, Charge Pumps, Energy Scavenging.	1
2	**Module II (10 Hrs)**	
2.1	**Delay Models**:	
	Introduction, Definitions, Timing Optimization.	1
	RC Delay Model: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits.	1
	Elmore Delay, Layout Dependence of Capacitance, Determining Effective Resistance.	1
	Linear Delay Model: Logical Effort, Parasitic Delay, Delay in a Logic Gate.	1
	Logical Effort of Paths: Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Example.	1

2.2	**Interconnect:**	
	Introduction, Wire Geometry, Interconnect Modelling: Resistance, Capacitance, Inductance (Pi modelling).	1
	Interconnect Impact: Delay, Energy, Crosstalk, Effective Resistance and Elmore Delay.	1
2.3	**Clocks:**	
	Clock System Architecture, Global Clock Generation, Global Clock Distribution	1
	Local Clock Gaters, Adaptive Deskewing, PLLs and DLLs.	1
2.4	**I/O:**	
	Basic I/O Pad Circuits, Electrostatic Discharge Protection.	1
3	**Module III (7 Hrs)**	
3.1	**Combinational Circuit Design:**	
	Static CMOS circuits, Combinational logic circuits	1
	Ratioed Circuits	1
3.2	**Dynamic logic:**	
	Domino Logic, Dual-Rail Domino Logic, Keepers	2
	Multiple-Output Domino Logic (MODL), NP Domino logic (NORA).	1
3.3	**BiCMOS logic gates**:	
	Inverter, NAND, NOR.	1
	Introduction to **Silicon-On-Insulator Circuit Design**	1
4	**Module IV (8 Hrs)**	
4.1	**Sequential Circuit Design:**	
	Sequencing Static Circuits-Flip-flops and latches**.**	1
4.2	**Sequencing Methods:**	
	Max-Delay Constraints	1
	Min-Delay Constraints	1
	Time Borrowing	1
	Clock Skew	1
4.3	**Circuit Design of Latches and Flip-Flops:**	
	Conventional CMOS Latches	1
	Conventional CMOS Flip-Flops	1
	True Single-Phase-Clock (TSPC) Latches and Flip-Flops.	1

5	**Module V (8 Hrs)**	
	Data path Subsystems:	
5.1	**Adders:**	

	Single-Bit Addition, Carry-Propagate Addition, Multiple-Input Addition	1
5.2	**Multipliers:**	
	Unsigned Array Multiplication, Booth Encoding	1
5.3	**Shifters:** Funnel Shifter, Barrel Shifter	1
5.4	**Comparators:** Magnitude Comparator	1
5.5	**Counters:** Binary Counters	1
5.6	**Designing of memory and array structures:**	
	SRAM	1
	DRAM and Embedded DRAM	1
	Read-Only Memory	1

Reference Books

1. Weste and Harris, CMOS VLSI Design A Circuits and Systems Perspective, 4/E, Pearson Education**.**
2. Weste and Harris, "Integrated Circuit Design", 4/e, 2011, Pearson Education**.**
3. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits, 3/e, Tata McGraw-Hill Education, 2003.
4. Rabaey, Chandrakasan and Nikolic, "Digital Integrated Circuits – A Design Perspective", 2/e, Pearson Education.
5. R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS, Circuit Design, Layout, and Simulation", 3/e, Wiley Interscience.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1TEC007	FPGA BASED SYSTEM DESIGN	PROGRAM CORE 2	3	0	0	3

Preamble: The purpose of this course is to introduce basic concepts of FPGA based system design and to impart practical skills in developing a synthesizable digital sub system using Verilog HDL.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Apply verilog programming to develop and simulate digital sub systems.**(Cognitive Knowledge Level: Apply)**
CO 2	Design RT-level combinational and regular sequential circuits **(Cognitive Knowledge Level: Create)**
CO 3	Construct FSM and FSMD**(Cognitive Knowledge Level: Analyse)**
CO 4	Analyse and implement UART subsystems in FPGA **(Cognitive Knowledge Level: Evaluate)**
CO 5	Explain architecture and features of programmable logic devices**(Cognitive Knowledge Level: Analyse)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.

PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2		3	2	2	1		1	1
CO 2	3		3	3	2	1		2	1
CO 3	1		2	3	2	1		1	2
CO 4			2	3	2	1		1	3
CO 5	2		3	3	3	1		2	

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination(%)
Apply	30	40
Analyse	30	35
Evaluate	25	25
Create	15	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 20 marks

Course based task/Seminar/Quiz : 10 marks

Test paper, 1 no. : 10 marks

The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Syllabus

Module 1 (Verilog HDL – based design, Overview of FPGA and EDA software)

Introduction, General description,Basic lexical elements and data types, Data types, Program skeleton,Structural description, Gate-level combinational circuit, Testbench, Introduction and overview of a general FPGA device,Overview of the Digilent S3 board, Development flow, Overview of the digital design tool (Vivado/ Xilinx ISE/any other open software) Suggested experiments- Gate-level greater-than circuit, Gate-level binary decoder

Module 2 (RT-level combinational circuit and Regular sequential circuit)

Introduction, Operators, Always block for a combinational circuit, if statement, Case statement, General coding guidelines for an always block, Parameter and constant, Design examples: shift register, Binary counters, Introduction to Regular Sequential Circuit, HDL code of the FF and register, Test bench for sequential circuits, Case study.

Module 3 (FSM & FSMD)

FSM: Introduction, FSM representation and code development, Mealy and Moore outputs, Design examples.

FSMD-Introduction, ASMD chart,Code development of an FSMD,Design examples

Module 4 (Implementation of UART sub system)

Introduction, UART receiving subsystem, UART transmitting subsystem, Overall UART system

Micro project-Full-featured UART, UART with an automatic baud rate detection circuit, UART with an automatic baud rate and parity detection circuit, UART-controlled stopwatch, UART-controlled rotating LED banner.

Module 5 (External SRAM and Programmable logic devices)

External SRAM:Introduction, Specification of the IS61LV25616AL SRAM, Basic memory controller, a safe design.

Programmable logic Devices:ROM,PLA,PAL,CPLD, FPGA Features, Limitations, Architectures.

Reference Books

1. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008
2. FPGA-Based System Design –WayneWolf,Verlag:PrenticeHall
3. ModernVLSI Design:System-on-Chip Design(3rdEdition)WayneWolf,Verlag
4. Field Programmable Gate Array Technology-S.Trimberger,Edr,1994,KluwerAcademic
5. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall
6. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", SecondEdition, Prentice Hall PTR, 2003
7. B. Bala Tripura Sundari, T. R. Padmanabhan, "Design Through Verilog HDL", WileyIndia, 2012

Model Question Paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ1TEC007 Course

Name: FPGA Based System Design

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Write Verilog code for 2 bit Gate-level greater than circuit.
2. Design a 2 bit priority encoder.
3. Design a Moore based rising edge detector.
4. Draw the conceptual block diagram of a UART receiving subsystem.
5. Differentiate PLA with PAL.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Write a verilog code for N-bit free running shift register.
7. Design a Fibonacci number circuit using Verilog.
8. Design a stopwatch which displays the time in three decimal digits and counts from 00.0 to 99.9 seconds and wraps
9. Design a UART receiver with 9600 baudrate and 25MHZ clock using Verilog;
10. Draw the block diagram, ASMD chart and develop Verilog code of SRAM controller.
11. Design the function F=XYZ'+Y'Z+XY' using PLA.
12. Design a debouncing circuit with RT methodology

(5x7=35 Marks

No	Topic	No. of Lectures
1	**Verilog HDL – based design, Overview of FPGA and EDA software**	**8 hours**
1.1	Introduction, General description, Basic lexical elements and data types, Data types,	2
1.2	Program skeleton, Structural description,	2
1.3	Gate-level combinational circuit, Test bench,	1
1.4	Introduction and overview of a general FPGA device,Overview of the Digilent S3 board,	1
1.5	Development flow, Overview of the digital design tool (Vivado/ Xilinx ISE/any other open software)	1
1.6	Suggested experiments- Gate-level greater-than circuit, Gate-level binary decoder	1
2	**RT-level combinational circuit and Regular sequential circuit**	**8 hours**
2.1	Introduction, Operators, Always block for a combinational circuit	1
2.2	if statement, Case statement,	1
2.3	General coding guidelines for an always block, Parameter and constant	1
2.4	Design examples : shift register, Binary counters	2
2.5	Introduction to Regular Sequential Circuit, HDL code of the FF and register	1
2.6	Testbench for sequential circuits, Case study	2
3	**FSM & FSMD**	**8 hours**
3.1	FSM: Introduction, FSM representation and code development	2
3.2	Mealy and Moore outputs,Design examples.	2
3.3	FSMD-Introduction, ASMD chart	2
3.4	Code development of an FSMD, Design examples	2
4	**Implementation of UART sub system**	**8 hours**
4.1	Introduction, UART receiving subsystem	1
4.2	UART transmitting subsystem, Overall UART system	1
4.3	Micro project-Full-featured UART, UART with an automatic baud rate detection circuit, UART with an automatic baud rate and parity detection circuit, UART-controlled stopwatch, UART-controlled rotating LED banner.	6
5	**External SRAM and Programmable logic devices**	**8 hours**
5.1	External SRAM: Introduction, Specification of the	1

	IS61LV25616AL SRAM	
5.2	Basic memory controller, a safe design.	1
5.3	Programmable logic Devices: ROM, PLA, PAL, CPLD	3
5.4	FPGA Features, Limitations, Architectures.	3
	Total	**40**

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1RGE100	RESEARCH METHODOLOGY AND IPR		2	0	0	2

Preamble: This course introduces the strategies and methods related to scientific research. The students are also trained in the oral presentation with visual aids and writing technical thesis/reports/research papers. The salient aspects of publication and patenting along with the crucial role of ethics in research is discussed.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Approach research projects with enthusiasm and creativity.
CO 2	Conduct literature survey and define research problem
CO 3	Adopt suitable methodologies for solution of the problem
CO 4	Deliver well-structured technical presentations and write technical reports.
CO 5	Publish/Patent research outcome.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	3	2	-	-	-	-	-
CO 2	3	2	-	-	-	-	-
CO 3	3	2	-	-	2	-	-
CO 4	3	3	2	-	-	-	-
CO 5	3	3	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	70 %
Analyse	30 %
Evaluate	
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Course based task: 15 marks

Some sample course based tasks that can be performed by the student given below.

- *Conduct a group discussion based on the good practices in research.*
- *Conduct literature survey on a suitable research topic and prepare a report based on this.*

Seminar: 15 marks

Test paper: 10 marks

End Semester Examination Pattern:

Total Marks: 60

The examination will be conducted by the respective college with the question provided by the University. The examination will be for 150 minutes and contain two parts; Part A and Part B. Part A will contain 6 short answer questions with 1 question each from modules 1 to 4, and 2 questions from module 5. Each question carries 5 marks. Part B will contain only 1 question based on a research article from the respective discipline and carries 30 marks. The students are to answer the questions based on that research article.

Sample question for part B is given below:

PART B			
7		Read the given article and write a report that addresses the following issues (The article given can be specific to the discipline concerned)	**Marks**
	a	What is the main research problem addressed?	**4**
	b	Identify the type of research	**4**
	c	Discuss the short comings in literature review if any?	**4**
	d	Discuss the significance of the study	**6**
	e	Discuss appropriateness of the methodology used for the study	**6**
	f	Summarize the important results and contributions by the authors	**6**

No	Topic	No. of Lectures
1	**Introduction**	
1.1	Meaning and significance of research, Skills, habits and attitudes for research, Types of research,	1
1.2	Characteristics of good research, Research process	1
1.3	Motivation for research: Motivational talks on research: "You and Your Research"- Richard Hamming	1
1.4	Thinking skills: Levels and styles of thinking, common-sense and scientific thinking, examples, logical thinking, division into sub-problems, verbalization, awareness of scale.	1
1.5	Creativity: Some definitions, illustrations from day to day life, intelligence versus creativity, creative process, requirements for creativity	1
2	**Literature survey Problem definition**	
2.1	Information gathering – reading, searching and documentation; types of literature. Journal index and impact factor.	1
2.2	Integration of research literature and identification of research gaps	1
2.3	Attributes and sources of research problems; problem formulation, Research question, multiple approaches to a problem	1
2.4	Problem solving strategies – reformulation or rephrasing, techniques of representation, Importance of graphical representation; examples.	1
2.5	Analytical and analogical reasoning, examples; Creative problem solving using Triz, Prescriptions for developing creativity and problem solving.	1
3	**Experimental and modelling skills**	
3.1	Scientific method; role of hypothesis in experiment; units and dimensions; dependent and independent variables; control in experiment	1
3.2	precision and accuracy; need for precision; definition, detection, estimation and reduction of random errors; statistical treatment of data; definition, detection and elimination of systematic errors;	1
3.3	Design of experiments; experimental logic; documentation	1
3.4	Types of models; stages in modelling; curve fitting; the role of approximations; problem representation; logical reasoning; mathematical skills;	1
3.5	Continuum/meso/micro scale approaches for numerical simulation;	1

	Two case studies illustrating experimental and modelling skills.	
4	**Effective communication - oral and written**	
4.1	Examples illustrating the importance of effective communication; stages and dimensions of a communication process.	1
4.2	Oral communication –verbal and non-verbal, casual, formal and informal communication; interactive communication; listening; form, content and delivery; various contexts for speaking-conference, seminar etc.	1
4.3	Guidelines for preparation of good presentation slides.	1
4.4	Written communication - form, content and language; layout, typography and illustrations; nomenclature, reference and citation styles, contexts for writing – paper, thesis, reports etc. Tools for document preparation-LaTeX.	1
4.5	Common errors in typing and documentation	1
5	**Publication and Patents**	
5.1	Relative importance of various forms of publication; Choice of journal and reviewing process, Stages in the realization of a paper.	1
5.2	Research metrics-Journal level, Article level and Author level, Plagiarism and research ethics	1
5.3	Introduction to IPR, Concepts of IPR, Types of IPR	1
5.4	Common rules of IPR practices, Types and Features of IPR Agreement, Trademark	1
5.5	Patents- Concept, Objectives and benefits, features, Patent process – steps and procedures	2

Reference Books

1. E. M. Phillips and D. S. Pugh, "How to get a PhD - a handbook for PhD students and their supervisors", Viva books Pvt Ltd.
2. G. L. Squires, "Practical physics", Cambridge University Press
3. Antony Wilson, Jane Gregory, Steve Miller, Shirley Earl, Handbook of Science Communication, Overseas Press India Pvt Ltd, New Delhi, 1st edition 2005
4. C. R. Kothari, Research Methodology, New Age International, 2004
5. Panneerselvam, Research Methodology, Prentice Hall of India, New Delhi, 2012.
6. Leedy P. D., Practical Research: Planning and Design, McMillan Publishing Co.
7. Day R. A., How to Write and Publish a Scientific Paper, Cambridge University Press, 1989.
8. William Strunk Jr., Elements of Style, Fingerprint Publishing, 2020
9. Peter Medawar, 'Advice to Young Scientist', Alfred P. Sloan Foundation Series, 1979.
10. E. O. Wilson, Letters to a Young Scientist, Liveright, 2014.
11. R. Hamming, You and Your Research, 1986 Talk at Bell Labs.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1LEC003	DESIGN LAB I	LABORATORY 1	0	0	2	1

Preamble: The purpose of this course is to provide a solid foundation that furnishes the learner with in-depth knowledge of VLSI design. The students will be able to study and practice various tools for the VLSI design and FPGA programming. They can find solutionsto real-world problems by completing this course in which they will be exposed to various hardware platforms and development boards and software tools for design, synthesis and simulation. This course covers architecture, programming, tools for development, testing and debugging and application notes. This course helps the learner to design an VLSI system as per the requirement and implement it with a professional grade tool.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Study of HDL and various VLSI design tools. **(Cognitive Knowledge Level: Analyse)**
CO 2	Analyse a problem statement and design a solution based on the available tools and find results. **(Cognitive Knowledge Level: Analyse)**
CO 3	Design and synthesis HDL codes for combinational circuits. **(Cognitive Knowledge Level: Evaluate)**
CO 4	Design and synthesis HDL codes for sequential circuits. **(Cognitive Knowledge Level: Evaluate)**
CO 5	Identify a practical problem and develop a solution, test and simulate using the available VLSI platform. **(Cognitive Knowledge Level: Create)**
CO6	Study, design and analyse analog VLSI circuits. **(Cognitive Knowledge Level: Evaluate)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.

PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1			2	2	1	1		1	1
CO 2	2		2	2	3	1		2	1
CO 3			2		1	1		2	1
CO 4			2		1	1		2	2
CO 5	2	3	2	2	3	2	3	2	1
CO 6			2	2	1	1		1	1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation
Apply	20
Analyze	20
Evaluate	20
Create	40

Mark distribution

Total Marks	Continuous Internal Evaluation	End Semester Examination
100	100	--

Continuous Internal Evaluation Pattern (Laboratory):

The laboratory courses will be having only Continuous Internal Evaluation and carry 100 marks. The final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

List of Experiments

The following experiments are to be completed by designing a solution for the problem in software or hardware. The solution may be tested and debugged so that it can be implemented in real time. Minimum of fifteen experiments are to be completed.

So No	Experiment Title	CO Mapping
1	Write HDL codes to find the highest number among three 4-bit numbers and demonstrate it using software simulation or hardware implementation.	CO1, CO2
2	Write HDL codes to design 8 bit adder using instantiation and demonstrate it using software simulation or hardware implementation.	CO1, CO2
3	Write HDL codes to design controller for 4*4 LED matrix and demonstrate it using software simulation or hardware implementation.	CO1, CO2
4	Write HDL codes to design D flipflop with reset and enable options and demonstrate it using software simulation or hardware implementation.	CO1, CO2
5	Write HDL codes to design register file using D flipflop and demonstrate it using software simulation or hardware implementation.	CO1, CO2
6	Write HDL codes to design 8 bit free running shift registers and demonstrate it using software simulation or hardware implementation.	CO1, CO2
7	Write HDL codes to design 8 bit universal shift registers and demonstrate it using software simulation or hardware implementation.	CO1, CO2
8	Write HDL codes to design 4 bit binary counter and demonstrate it using software simulation or hardware implementation.	CO1, CO2
9	Write HDL codes to design 4 bit universal binary counter and demonstrate it using software simulation or hardware implementation.	CO1, CO2
10	Write HDL codes to design a sequence detector using software simulation or hardware implementation.	CO1, CO2
11	Write HDL codes to design a four-bit array multiplier using software simulation or hardware implementation.	CO1, CO2
12	Write HDL codes to design an 8-bit ALU using software simulation or hardware implementation.	CO3

13	Write HDL codes to design 8-bit johnson and ring counters using software simulation or hardware implementation.	CO4
14	Write HDL codes to design 4-bit PISO and PIPO shift registers using software simulation or hardware implementation.	CO4
15	Write HDL codes to design a MAC using software simulation or hardware implementation	CO3
16	rite HDL codes to design an 8-bit RAM/ROM using software simulation or hardware implementation.	CO3
17	Implement an SOP/POS function using HDL.	CO5
18	Write HDL to realise higher order Multiplexers and demultiplexers using software simulation or hardware implementation.	CO5
19	Write HDL codes to realize encoders and decoders using software simulation or hardware implementation.	CO5
20	Analog Experiments 1. MOSFET VI Characteristics 2. CMOS based NAND and NOR circuits	CO6

Reference

1. J.Bhaskar, " VHDL Primer",Pearson Education India; 3rd edition (1 January 2015)
2. J.Bhaskar,"A VHDL Synthesis Primer",Pearson Education, Second Edition
3. Charles H. Roth, Jr., Lizy K. John,"Digital Systems Design Using VHDL", 3rd Edition,Cengage Learning
4. Stephen Brown , Zvonko Vranesic ,Fundamentals of Digital Logic with VHDL Design",McGraw Hill Education; 3rd edition (1 July 2017)
5. Pedroni VA,"Circuit Design and Simulation With VHDL",Prentice Hall India Learning Private Limited; 2nd edition (1 January 2011)
6. Jan M Rabaey et al.,"Digital Integrated Circuits A design perspective", Pearson Education India; Second edition (25 May 2016)
7. Wolfe Wayne," FPGA-Based System Design",Prentice Hall Modern Semiconductor Design Series
8. https://www.xilinx.com/support/documentation-navigation/self-paced-tutorials/see-all-tutorials.htmls

SEMESTER I

PROGRAM ELECTIVE I

SLOT	SL NO	COURSE CODE	COURSE NAME	L-T-P	HOURS	CREDIT
D	1	24SJ1EEC034	PHYSICAL DESIGN AUTOMATION	3-0-0	3	3
	2	24SJ1EEC035	DESIGN WITH ADVANCED MICROCONTROLLER	3-0-0	3	3
	3	24SJ1EEC036	EDA TOOLS	3-0-0	3	3
	4	24SJ1EEC037	DSP ALGORITHMS AND ARCHITECTURE	3-0-0	3	3
	5	24SJ1EEC038	ADVANCED DIGITAL SIGNAL PROCESSING	3-0-0	3	3
	6	24SJ1EEC007	ELECTRONIC PACKAGING	3-0-0	3	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE C034	PHYSICAL DESIGN AUTOMATION	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: This course aims to familiarize various stages of VLSI Physical Design and algorithms used to automate the process.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply Search Algorithms and Shortest Path Algorithms to graphs representing VLSI problem formulations
CO 2	Outline VLSI Design Flow, Design Styles and Apply Partitioning Algorithms to graphs representation of circuits
CO 3	Illustrate Layout Design Rules and Apply different algorithms for layout compaction
CO 4	Make use of different concepts in Floor plan, Placement and Pin Assignment to Apply suitable algorithms for finding solutions
CO 5	Understand Routing strategies and Apply algorithms to solve Routing requirements.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	1	2	2				1	2	1
CO 2	2			1	2	1		2	1
CO 3	1	2		1	1	2	1	2	1
CO 4								2	1
CO 5	1							1	1

Assessment Pattern

Bloom's Category	End Semester Examination(%)
Apply	40
Analyse	50
Evaluate	10
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No.: 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question carry 7 marks.

Model Question Paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ1EEC034 Course

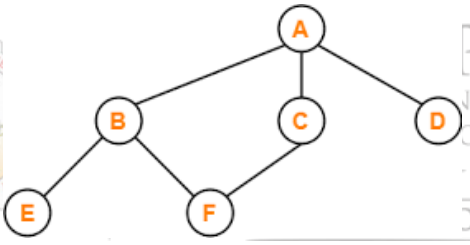
Name: Physical Design Automation

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Perform topological sorting on the following graph



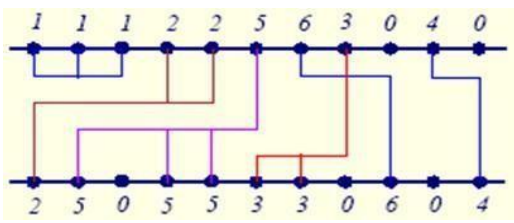
2. KL algorithm is an example of a balanced partitioning algorithm. Justify.

3. Can longest path algorithm for directed acyclic graphs (DAG) be used as an alternate for shortest path algorithm? If yes, suggest atleast two modifications.

4. Consider the floorplan given below, consisting of four leaf cells: A, B, C and D. Draw two slicing tree representations.

A	B
C	D

5. For the following Channel Routing problem, what is the channel density?

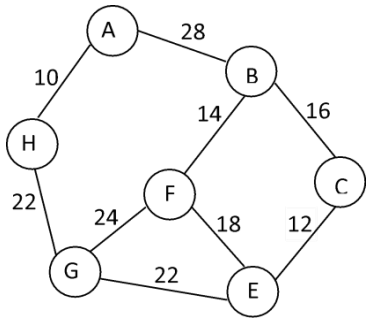


(5x5=25 Marks)

PART B

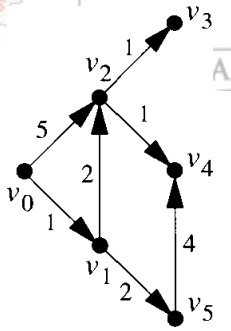
Answer any 5 questions. Each question carries 7 marks

6. Apply Dijkstra's Algorithm on the graph shown below to find shortest path to all vertices from the vertex H.

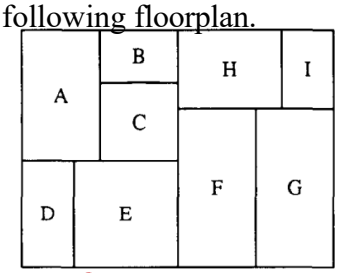


7. Draw the flowchart for VLSI Physical Design cycle.

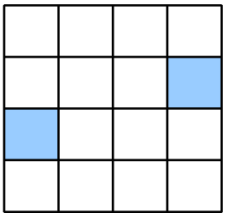
8. Apply Longest Path Algorithm to the following graph to find the longest path from V_0.



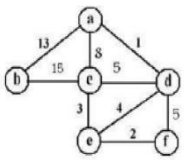
9. Draw the Vertical and Horizontal Constraint Graph for the following floorplan.



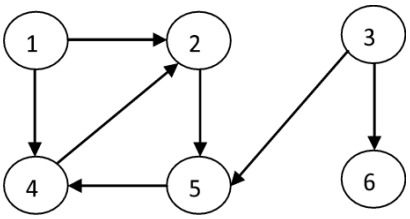
10. Apply Lee's Algorithm to find shortest routing path from S to T.



11. Apply Prim's algorithm to find the minimum spanning tree of the graph shown below



12. Consider the graph G(V, E) shown below. Assume 1 is the starting node.



Perform Depth First Search and Breadth First Search on the above graph.

Syllabus

Module 1 Graph Terminology, Search Algorithms and Shortest Path Algorithms

Basic graph theory terminology, Data structures for representation of Graphs – Adjacency Matrix, Adjacency List, Breadth First Search, Depth First Search, Topological Sort, Breadth First Search, Depth First Search, Topological Sort, Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path, Prim's Algorithm for Minimum Spanning Tree

Module 2 Design Automation and Partitioning Algorithms

VLSI Design Flow, Physical Design Flow, VLSI Design Styles, Terminology, Optimization Goals, Levels of Partitioning, Parameters for Partitioning, Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm

Module 3 Layout Compaction

Layout Layers and Design Rules, Physical Design Optimizations, Applications of Compaction, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path Algorithm for DAGs, Longest Path in Graph with Cycles - Liao-Wong Algorithm

Module 4 Floorplanning, Placement and Pin Assignment

Optimization Goals, Slicing Floorplan, Non-Slicing Floorplan, Constraint Graphs, Conversion of Floorplan to a Constraint Graph Pair, Floorplan Sizing, Shape Functions, Corner Points, Minimum Area Algorithm, Optimization Objectives, Wirelength Estimation,

Weighted Wirelength, Maximum Cut Size, Wire Density, Concentric Circle Method, Topological Pin Assignment

Module 5 Routing

Terminology and Definitions, Optimization Goals, Representation of Routing Regions, Area Routing, Lee's Algorithm, Hadlock Algorithm, Channel Routing, Horizontal and Vertical Constraint Graph, Left-Edge algorithm

Course Plan

No	Topic	No. of Lectures
1	**Graph Terminology, Search Algorithms and Shortest Path Algorithms**	
1.1	Basic graph theory terminology, Data structures for representation of Graphs – Adjacency Matrix, Adjacency List	2
1.2	Breadth First Search, Depth First Search, Topological Sort	3
1.3	Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path, Prim's Algorithm for Minimum Spanning Tree	3
2	**Design Automation and Partitioning Algorithms**	
2.1	VLSI Design Flow, Physical Design Flow, VLSI Design Styles	3
2.2	Terminology, Optimization Goals, Levels of Partitioning, Parameters for Partitioning	2
2.3	Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm	4
3	**Layout Compaction**	
3.1	Layout Layers and Design Rules, Physical Design Optimizations	2
3.2	Applications of Compaction, Graph Theoretical Formulation, Maximum Distance Constraints	2
3.3	Longest Path Algorithm for DAGs, Longest Path in Graph with Cycles -Liao-Wong Algorithm	4
4	**Floorplanning, Placement and Pin Assignment**	
4.1	Optimization Goals, Slicing Floorplan, Non-Slicing Floorplan, Constraint Graphs, Conversion of Floorplan to a Constraint Graph Pair	3
4.2	Floorplan Sizing, Shape Functions, Corner Points, Minimum Area Algorithm	3
4.3	Optimization Objectives, Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density	1
4.4	Concentric Circle Method, Topological Pin Assignment	1
5	**Routing**	
5.1	Terminology and Definitions, Optimization Goals, Representation of Routing Regions	1
5.2	Area Routing, Lee's Algorithm, Hadlock Algorithm	3
5.3	Channel Routing, Horizontal and Vertical Constraint Graph, Left-Edge algorithm	3
	Total	40

Reference Books

1. Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2011th edition.
2. Gerez,Sabih H., “Algorithms for VLSI Design Automation”, John Wiley & Sons, 2006.
3. Sherwani, Naveed A., “Algorithms for VLSI Physical Design Automation”, Kluwer Academic Publishers, 1999.
4. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "Introduction to Algorithms." The MIT Press, 3rd edition, 2009.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EEC 101	ADVANCED DIGITAL SYSTEM DESIGN	PROGRAM ELECTIVE 2	3	0	0	3

Preamble:

- The student will learn analysis and synthesis of combinational and sequential circuits.
- Learn the principles of digital design and practices using data path components such as counters, shift registers, and adders etc.
- To introduce Register Transfer Level (RTL) design.
- The student will learn about optimizations and trade-offs in combinational logic, sequential logic, data path component and RTL design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Create and analyze combinational and sequential circuits.
CO 2	Design circuits using data path components such as counters, shift registers, adders etc.
CO 3	Analyze Synchronizer Failure and Metastability
CO 4	Understand Register Transfer Level (RTL) design
CO 5	Understand optimizations and trade-offs in combinational logic, sequential logic, data path components and RTL design

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.

PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2	2	2	2		2		1	2
CO 2	2	2	1	1		2	1	2	2
CO 3	1		1	1	2	2		2	1
CO 4	2	1					1	2	2
CO 5			1	1			1	1	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40%
Analyse	40%
Evaluate	20%
Create	-

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed Original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Micro project : 15 marks

Test paper, 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

End Semester Examination: 60 marks

The end semester examination will be conducted by the respective College.

There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL INSTITUTE

FIRST SEMESTER M.TECH DEGREE EXAMINATION DECEMBER 20XX

ELECTRONICS AND COMMUNICATION ENGINEERING 24SJ1EEC101

ADVANCED DIGITAL SYSTEM DESIGN

Time: 2.5 hrs. Max. Marks: 60

Answer all questions (5 marks each)

1. Design a circuit, using four registers, that stores the four values present at an 8 bit input D during the previous four clock cycles. The circuit should have a single 8-bit output that can be configured using two inputs s1 and s0 to output any one of the four registers (hint: use an 8-bit 4 x 1 mux)
2. Design a 4-bit register with 2 control inputs s1 and s0, 4 data inputs I3, I2, I1 and I0 and 4 data outputsQ3, Q2, Q1 and Q0. When s1s0 = 00, the register maintains it's value. When s1s0 = 01, the register loads I3..I0. When s1s0 = 10, the register clears itself to 0000. When s1s0 = 11, the register reverses it's bits, so 1110 would become 0111, and 1010 would become 0101
3. Write notes on synchronous failure
4. Compose a 2048 x 8 ROM using only 256 x 8 ROMs
5. For the function F(a,b,c) = a'c + ac + a'b, determine all prime implicants and all essential prime implicants: using the tabular method.

Answer any 5 questions (7 marks each)

6. Draw a state diagram for an FSM that has an input X and an output Y. Whenever X changes from 0 to 1, Y should become 1 for two clock cycles and then return to 0- even if X is still 1. (Assume that an implicit rising clock is ANDed with every FSM transition condition.)

7. Design a 4-bit up-counter that has two control inputs: cnt enables counting up, while clear synchronously resets the counter to all 0s:
(a) using parallel load register as a building block,
(b) using flip-flops and muxes

8. Write notes on clock skew

9. Use the RTL design process to create a 4-bit up-counter with input cnt (1 means count up), clear input clr, a terminal count output tc, and a 4-bit output Q indicating the present count.

10. Compare different types of memory. Describe various types of ROM?
11. Discuss various methods of state encoding with examples.
12. Explain the different optimizations and trade-offs implemented in RTL design with examples.

Syllabus

Module 1

Combinational Logic Design Principles: Switching Algebra. Combinational-Circuit Analysis, Combinational- Circuit Synthesis. Programmed Minimization Methods, Timing Hazards, Sequential Logic Design Principles : Latches, flip flops, timing and glitches, Finite State Machines, Standard Controller Architecture for Implementing an FSM as a Sequential Circuit

Module 2

Combinational Circuit Documentation Standards, Datapath Components: Registers, Adders Comparators, Multiplier—Array-Style, Subtractors and Signed Number, Arithmetic- Logic Units—ALUs, Shifters, Counters and Timers, Register Files

Module 3

Synchronous Design Methodology- synchronous system structure, Impediments to Synchronous Design: clock skew, gating the clock synchronizer failure, asynchronous inputs,

Synchronizer Failure and Metastability, Reliable synchronizer design, Analysis of metastable timing, better synchonizers

Module 4

Register-Transfer Level (RTL) Design: High-Level State Machine, RTL Design Process, Determining Clock Frequency, Behavioural-Level Design: C to Gates, Memory Components, Queues, FIFOs, Multiple Processors

Module 5

Optimizations and Tradeoffs: Combinational Logic Optimizations and Tradeoffs, Sequential Logic Optimizations and Tradeoffs, Data path Component Tradeoffs, RTL Design Optimizations and Tradeoffs

No	Topic	No. of Lectures
1	**Module 1**	
1.1	**Combinational Logic Design Principles**	
1.1.1	Switching Algebra	0.5
1.2	Combinational-Circuit Analysis	0.5
1.3	Combinational- Circuit Synthesis	1
1.3.1	Programmed Minimization Methods	1
1.4	Timing Hazards	1
1.5	**Sequential Logic Design Principles**	
1.5.1	Latches, flip flops, timing and glitches	2
1.5.2	Finite State Machines	1
1.5.3	Standard Controller Architecture for Implementing an FSM as a Sequential Circuit	1
2	**Module 2**	
2.1	**Combinational Circuit Documentation Standards**	
2.1.1	Combinational Circuit Documentation Standards	1
2.2	**Datapath Components:**	
2.2.1	Registers, Adders	1
2.2.2	Comparators, Multiplier—Array-Style	2
2.2.3	Subtractors and Signed Number, Arithmetic- Logic Units—ALUs	2
2.2.4	Shifters, Counters and Timers, Register Files	2
	Module 3	
3.1	**Synchronous Design Methodology**	
3.1.1	synchronous system structure	1
3.2	**Impediments to Synchronous Design:**	

3.2.1	clock skew	1
3.2.2	gating the clock synchronizer failure,	1
3.2.3	asynchronous inputs	1
3.3	**Synchronizer Failure and Metastability,**	
3.3.1	Synchronizer Failure, Reliable synchronizer design	2
3.3.2	Analysis of metastable timing, Better synchonizers	2
	Module 4	
4.	**Register-Transfer Level (RTL) Design**:	
4.1	High-Level State Machine,	2
4.2	RTL Design Process, ,	2
4.3	Determining Clock Frequency	1
4.4	Behavioural-Level Design: C to Gates,	0.5
4.5	Memory Components, Queues- FIFOs,	2
4.6	Multiple Processors	0.5
	Module 5	
5	Optimizations and Tradeoffs:	
5.1	Combinational Logic Optimizations and Tradeoffs	2
5.2	Sequential Logic Optimizations and Tradeoffs	2
5.3	Data path Component Tradeoffs	2
5.4	RTL Design Optimizations and Tradeoffs	2

References:

1. Frank Vahid, "Digital Design with RTL Design, VHDL and Verilog", 2/e, Wiley, 2010.
2. Harris & Harris, "Digital Design and Computer Architecture", 2/e, Morgan Kaufmann, 2012.
3. John F. Wakerly, "Digital Design Principles and Practices", 4/e, Prentice Hall, 2005.
4. William James Dally, R. Curtis Harting, "Digital Design: A Systems Approach", Cambridge Institute Press, 2012.
5. Randy H. Katz and Gaetano Borriello , "Contemporary Logic Design", 2/E, Prentice Hall India, 2009.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EEC036	EDA TOOLS	PROGRAM ELECTIVE 1	3	0	0	3

Preamble:

1. To understand the basic methodology of Digital and Analog system design.
2. To know the EDA tool concepts used for electronic system design for ICs.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	Apply the design methodology of EDA for Digital Simulation
CO 2	Analyse the Synthesis steps of Digital circuits for optimal performance
CO 3	Evaluate the architectures for testing and testability of Digital circuits
CO 4	Evaluate the libraries for Digital circuits, create the layouts for the circuits and evaluate the verification method
CO 5	Analyse the analog and mixed signal simulation methods

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2	2	2	2	1	2		1	2
CO 2	2	2	1	1		2	1	2	2
CO 3			1	1	2	2		2	2
CO 4	2	1					1	2	1
CO 5			1	1			1	1	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	19/60 32%
Analyse	13/60 22%
Evaluate	32/60 53%
Create	0/60 0

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ Abdul Kalam Technological Institute

First Semester M.Tech Degree Examination December 20xx

ELECTRONICS AND COMMUNICATION ENGINEERING

Answer all Questions: 5 marks each – 5 x 5 = 25 marks

1. Using the example of a multiplier evaluate the differences between algorithmic and RTL level descriptions for Integrated chips.
2. Evaluate the steps for logical synthesis? With the help of the below codes discuss the differences in the synthesized code.

```
...
c := a + b;
d := a - b;
IF(sub = '1')
THEN
   result <= d;
ELSE
   result <= c;
END IF;
```

```
...
IF(sub = '1')
THEN
   b := - b;
END IF;

result <= a + b;
```

Fig 1.

3. Apply the SDF format for standardized digital models? Make a comparison with Explain Timing Back Annotation with a neat diagram?
4. How does optimization constraints such as time affect the delay and area of a chip? Give graphs to evaluate your argument.
5. Analyse synopsys design rule and optimization constraints related to area, delay and timing.

Answer any 5 Questions: 7 marks each – 5 x 7 = 35 marks

6. Giving a block diagram , analyse the structure of a Digital simulator? What are the logic values associated with the simulator? Briefly discuss the functional simulation of the following circuit:

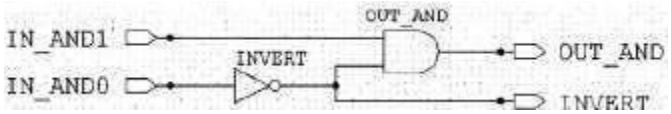


Fig 2.

7. Evaluate the Model checking method of formal verification to prove the correctness of a circuit s=a+b+c+d for non negative binary numbers of length n bits? Use a 4 to 2 reduction circuit for the verification method?
8. Differentiate the concepts of fault collapsing and dominance with an example?

9. Evaluate the geometric layout methods giving the example of an Inverter circuit? Give a definition for LVS? What are the rules followed for DRC?

10. By giving a neat diagram evaluate the simultaneous controllability and observability by means of scan registers?

11. Discuss the construction of Standard cells for Digital library? How are the cells characterized?

12 Explain with neat diagram the Boundary scan standards to address the board level testing?

Syllabus

No	Topic	No. of Hours
1	**Concepts of EDA:** Design Methodology Development steps - algorithmic model, register transfer level, logic design, transistor level circuit design, polygon pushing, design for test Implementation flow Top down vs Bottom up design process Application specific integrated circuits – design goals, design styles Design Libraries - Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries	8
No	**Topic**	**No. of Hours**
2	**Simulations:** **Digital Simulation :** Why?, Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation. **Analog Simulation:** Spice concept, Spice transistor models, Models of Operational Amplifiers, Analysis of Loop gain as Stability Criterion of Analog Circuits. **Mixed Signal Simulation:** Overview, Simulation on different levels of abstraction, Concept of Mixed signal simulators	8
3	**Design for Testability Fundamentals:** Faults in Digital circuits and their modeling, Fault simulation and fault collapsing, Digital test pattern generation–ATPG, ATPG algorithms, ATPG-Vector Formats and Compaction and Compression. Scan Architectures- Testability, Scan Registers, Generic scan	9

	based designs, Boundary Scan-JTAG. Built in Self Test (BIST) - BIST concepts and test pattern generation Test pattern generation for Combinational Circuits Test pattern for Sequential Circuits	
4	**Synthesis and Formal Verification:** Synthesis - Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping. Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification.	8
No	**Topic**	**No. of Hours**
5	**Geometric Layout and Geometric Verification:** Layout of CMOS circuits: layers in CMOS layout, latch-up special requirements for analog layout, substrate noise Devices in CMOS : resistors, capacitors, diodes, BJT; Data formats: LEF Data format, GDSII Data format Standard cell Layout: standard cells, abstract view, floor planning, placement, routing **Geometric Verification:** Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS.	7

Reference Books

1. Jansen, Dirk,"The Electronic Design Automation Handbook", 2003.
2. MironAbramovici, Melvin A.Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
3. M.J.S.Smith.,"Application-Specific Integrated Circuits", Addison Wesley.
4. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits- a Design perspective", Pearson education/ Prentice-Hall India Ltd, 2nd edition.
5. M.H.Rashid,"SPICE FOR Circuits And Electronics Using PSPICE", Prentice Hall, 2nd edition

Course Plan (For 3 credit courses, the content can be for 40 hrs)

No	Topic	No. of Lectures
1	**Concepts of EDA**	
1.1	Design Methodology Development steps - algorithmic model, register transfer level, logic design, transistor level circuit design, polygon pushing, design for test	2

1.2	Implementation flow Top down vs Bottom up design process	2
1.2	Application specific integrated circuits – design goals, design styles	2
1.3	Design Libraries - Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries	2
2	**Simulations**	
2.1	**Digital Simulation :**Why?, Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation.	3
2.2	**Analog Simulation:** Spice concept, Spice transistor models, Models of Operational Amplifiers, Analysis of Loop gain as Stability Criterion of Analog Circuits.	3
2.3	**Mixed Signal Simulation:** Overview, Simulation on different levels of abstraction, Concept of Mixed signal simulators	2
3	**Design for Testability Fundamentals:**	
3.1	Faults in Digital circuits and their modeling, Fault simulation and fault collapsing,	2
3.2	Digital test pattern generation–ATPG, ATPG algorithms, ATPG-Vector Formats and Compaction and Compression.	2
3.3	Scan Architectures- Testability, Scan Registers, Generic scan based designs, Boundary Scan-JTAG.	2
3.4	Built in Self Test (BIST) - BIST concepts and test pattern generation	2
3.5	Test pattern generation for Combinational Circuits Test pattern for Sequential Circuits	1
4	**Synthesis and Formal Verification:**	
4.1	Synthesis - Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping.	4
4.2	Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification.	4
5	**Geometric Layout and Geometric Verification**	
5.1	Layout of CMOS circuits: layers in CMOS layout, latch-up special requirements for analog layout, substrate noise Devices in CMOS : resistors, capacitors, diodes, BJT; Data formats: LEF Data format, GDSII Data format	2
5.2	Standard cell Layout: standard cells, abstract view, floor planning, placement, routing	2
5.3	**Geometric Verification:** Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS.	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE C037	DSP ALGORITHMS AND ARCHITECTURE	PROGRAM ELECTIVE I	3	0	0	3

Preamble: This course aims to familiarize the architecture of different DSP processors and its implementation in real time applications. The course also analyses the concepts of pipelining and dynamic scheduling in DSP algorithms.

Course Outcomes: After the completion of the course, the student will be able to

CO 1	Have good understanding of the architecture of different processors
CO 2	Analyse the architecture of Blackfin and TMS320C64x processors
CO 3	Apply the concepts of pipelining & Dynamic scheduling
CO 4	Design FIR and IIR filter using different methods
CO 5	Interface the DSP processor in real time applications

Program Outcomes:

PO No:	Program Outcomes:
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	1	2	2	2		2		1	2
CO 2	1	1	1	2		2	1	2	2
CO 3	1		1	1	2	2		1	1
CO 4	2	1					1	2	1
CO 5			1	1			1	1	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	20
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M. TECH DEGREE EXAMINATION

Electronics & Communication Engineering

(Advanced Electronics & Communication Engineering)

24SJ1EEC037—DSP Algorithms and Architecture

Max. Marks: 60 Duration: 2.5 Hours

PART A

Answer All Questions

Each question carries 5 marks

1. What is superscalar processor? Explain its design characteristics.
2. Briefly explain the interrupts of DSP processor TMS320C64x.
3. Explain briefly the technique of reducing data hazards.
4. Derive the frequency warping equation, $\omega_s = \frac{2}{T}\tan\frac{\omega_d T}{2}$ $\omega_s = \frac{2}{T}\tan\frac{\omega_d T}{2}$.
5. Explain with the neat diagram the operation of pitch detector.

(5 x 5 = 25 marks)

PART B

Answer any 5 Questions. Each carries 7 marks

6. Explain briefly VLIW architecture, after drawing its schematic. Compare any 3 architecture characteristics of RISC, CISC and VLIW.
7. Explain the architecture of BLACKFIN processor, with the help of a neat block diagram.
8. Draw the block diagram of TMS320C64x architecture and briefly explain each block.

9. With the help of a block diagram explain branch optimized MIPS pipeline data path.

10. Illustrate Tomasulo's algorithm for dynamic scheduling, with the help of a neat block diagram.

11. Design a linear phase FIR low pass filter using rectangular window by taking 7 samples of window sequence and with a cut off frequency $\omega_c = 0.4\pi rad/sample$

$\omega_c = 0.4\pi rad/sample$

12. Explain the real time implementation of the processor TMS320C64X in an MP3 voice recorder–player, with neat schematics.

(5 x 7 marks = 35 marks)

SYLLABUS

Module :1

INTRODUCTION TO COMPUTER ARCHITECTURE:

Introduction, Role of computer architecture in daily life. Von Neumann versus Harvard Architecture, CISC & RISC Architecture. Architectures of superscalar and VLIW processors. Pipelined Superscalar processors and Comparison of CISC, RISC & VLIW.

Module :2

DETAILED ARCHITECTURE OF DIFFERENT PROCESSORS:

Introduction, Commercial digital Signal-processing Devices – Architecture Details of Black Fin processor (Analog Devices), Core processor interfacing, memory access & different operations performed by ALU. Architecture, Data Addressing Modes, Memory Space of TMS320C64x Processors, Program Control & On-Chip peripherals, Interrupts of DSP processor TMS320C64x. Applications of the above processors.

Module :3

CONCEPTS – PIPELINING & DYNAMIC SCHEDULING

Basic pipeline: Implementation details-pipeline hazards (based on MIPS 4000). Dynamic hardware prediction- Tomasulo's algorithm-Reducing data hazards and branch hazards. Multiple issue-hardware-based speculation.

Module :4

DIGITAL FILTER DESIGN & BILINEAR TRANSFORMATION:

Review of digital filter design: FIR & IIR filters – Difference equation and Transfer function Direct form I & II structures. Design example of FIR filter using window method. IIR filter design – Analog to digital transformation. Impulse Invariance and Bilinear transformation-Frequency warping. Example problems on IIR filter design.

Module :5

DSP PROCESSORS INTERFACING IN REAL TIME APPLICATIONS:

Introduction, Synchronous Serial Interface, CODEC Interface Circuit, DSP hierarchical memory architecture, programming optimization guidelines, Real-life applications using DSP TMS320C family-MP3 voice recorder–player, Bio-telemetry Receiver, Speech Processing System.

Reference Books

1. J. L. Hennesy, D.A. Patterson, "Computer Architecture A Quantitative Approach", 3/e, Elsevier India

2. Proakis, J.G. & Manolakis, D.G., "Digital Signal Processing: Principles, Algorithms & Applications", 3/e Prentice Hall of India, 1996.

3. Ifeachor, E.C. & Jervis, B.W., "Digital Signal Processing: A Practical Approach",2/e, Pearson Education Asia, 2002.

4. Nasser Kehtarnavaz, "Real Time Signal Processing Based on TMS320C6000", Elsevier, 2004.

Course Plan

No	Topic	No. of Lectures
1	**INTRODUCTION TO COMPUTER ARCHITECTURE: 8 hours**	
1.1	Introduction, Role of computer architecture in daily life.	1
1.2	Von Neumann versus Harvard Architecture, CISC & RISC Architecture.	3
1.3	Architectures of superscalar and VLIW processors.	2
1.4	Pipelined Superscalar processors and Comparison of CISC, RISC & VLIW	2
2	**DETAILED ARCHITECTURE OF DIFFERENT PROCESSORS: 8 hours**	
2.1	Introduction, Commercial digital Signal-processing Devices	1
2.2	Architecture Details of Black Fin processor (Analog Devices), Core processor interfacing, memory access & different operations performed by ALU.	2
2.3	Architecture of DSP processor TMS320C64x. Data Addressing Modes of TMS320C64x. Memory Space of TMS320C64x Processors, Program Control	3
2.4	On-Chip peripherals of TMS320C64x Processor Interrupts of TMS320C64x Processor, Applications of this processor	2
3	**CONCEPTS – PIPELINING & DYNAMIC SCHEDULING : 8 hours**	
3.1	Basic pipeline: implementation details-pipeline hazards (based on MIPS 4000)	2
3.2	Dynamic hardware prediction- Tomasulo's algorithm	3
3.3	Reducing data hazards and branch hazards	2

3.4	Multiple issue- hardware-based speculation	1
4	**DIGITAL FILTER DESIGN & BILINEAR TRANSFORMATION: 9 hours**	
4.1	Review of digital filter design: FIR & IIR filters – Difference equation and Transfer function Direct form I & II structures.	2
4.2	Design example of FIR filter using window method.	2
4.3	IIR filter design – Analog to digital transformation. Impulse Invariance and Bilinear transformation Frequency warping	3
4.4	Example problems on IIR filter design	2
5	**DSP PROCESSORS INTERFACING IN REAL TIME APPLICATIONS: 7 hours**	
5.1	Introduction, Synchronous Serial Interface, CODEC Interface Circuit	2
5.2	DSP hierarchical memory architecture, programming optimization guidelines	2
5.3	Real-life applications using DSP TMS320C family- MP3 voice recorder–player, Bio-telemetry Receiver, Speech Processing System.	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE G038	ADVANCED DIGITAL SIGNAL PROCESSING	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: Through this course students can understand discrete/ and Fast Fourier transforms in depth for signal analysis. Students are equipped to design appropriate digital filters for signal processing applications. Students will know about Model parameter estimation techniques. They will get familiarized with the fundamentals of multirate digital signalprocessing.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Get a deep knowledge of designing various filters for signal processing
CO 2	Study the algorithms used for signal processing
CO 3	Develop the capacity to propose better filter designs and algorithms for various applications
CO 4	Understand the theory of multi rate digital signal processing
CO 5	Familiarize the applications of signal processing in different domains

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1			3	3	3	1		1	
CO 2	1		3	3	2			1	1
CO 3	2		3	3	3	2		2	2
CO 4	1		2	2	2	1		1	1
CO 5	1		1		1			1	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40 %
Analyse	40 %
Evaluate	20 %
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed Original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Micro project : 15 marks

Test paper, 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

End Semester Examination: 60 marks

The end semester examination will be conducted by the respective College.

There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M. TECH DEGREE EXAMINATION

ELECTRONICS & COMMUNICATION ENGINEERING

24SJ1EEG038: ADVANCED DIGITAL SIGNAL PROCESSING

Max. Marks : 60 Duration: 2.5 Hour

PART A

Answer all questions (5 x 5 = 25 Marks)

1. With neat diagrams, explain the performance specifications of IIR filters? (5 Marks)
2. What are the practical limitations of the basic LMS algorithm? (5 Marks)
3. Describe the computational requirements for Bartlett power spectrum estimate. (5 Marks)
4. Discuss a method to decrease the sampling rate of a signal by an integer factor D. (5 Marks)
5. Explain the application of DSP in speech processing. (5 Marks)

PART B

Answer five questions, one question from each module (7 x 5 = 35 Marks)

6. An ideal high pass filter has a passband specified as, $\pi/4 \leq |\omega| \leq \pi$. Find the filter coefficients for the linear phase FIR filter with N = 11 (number of coefficients of the filter) using the Hanning window. (7 marks)
7. Explain the RLS adaptive algorithm. (7 marks)
8. What do you mean by periodogram? Explain the methods used for the computation of power density spectrum of random signals? (7 marks)
9. With the required expressions, illustrate how Reconstruction of the signal takes place in QMF Bank. (7 marks)
10. Explain the Wiener Filter based prediction algorithm. (7 marks)
11. Illustrate the use of Multirate digital signal processing in sub-band coding. (7 marks)
12. An ideal lowpass filter has a passband specified as, $-\frac{\pi}{2} \leq \left|H(e^{j\omega})\right| \leq \frac{\pi}{2}$.

    Find the filter coefficients, transfer function of realizable filter and magnitude of frequency response for the linear phase FIR filter with N = 11 (number of coefficients of the filter)? (7 marks)

Module 1: Review on digital signal processing basics

Review of Frequency and time domain analysis -Discrete Fourier Transforms.
Digital Filters-IIR Filters–Bilinear transformation , FIR filters– Windowing method, Finite wordlength effect Problems.

Module 2: Linear and Adaptive Filter Design

Linear prediction & optimum linear filters, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction, Adaptive Filters , Minimum mean square criterion.

Module 3: Power Spectrum Estimation

Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Estimation methods for AR model parameters. Non parametric spectrum estimation, Periodogram- Bartlett's method-Minimum variance estimation.

Module 4: Memory Test and Delay Test

Memory Faults, Fault Manifestations, Failure Mechanisms, March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects, Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies

Module 5: DFT and BIST

Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads of Scan Design, Partial-Scan Design, Variations of Scan, Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR, BIST Response Compaction using LFSR, Multiple Input Signature Register

Course Plan

No	Topic	No. of Lectures
1	**Review on digital signal processing basics**	**8 hours**
1.1	Review of Frequency and time domain analysis -Discrete Fourier Transforms	2
1.2	Digital Filters-IIR Filters–Bilinear transformation	2
1.3	FIR filters– Windowing method	2
1.4	Finite wordlength effect Problems	2
2	**Linear and Adaptive Filter Design**	**8 hours**
2.1	Linear prediction & optimum linear filters	2
2.2	AR Lattice and ARMA Lattice-Ladder Filters	2
2.3	Wiener Filters for Filtering and Prediction	1
2.4	Adaptive Filters	2
2.5	Minimum mean square criterion	1
3	**Power Spectrum Estimation**	**8 hours**

3.1	Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters	1
3.2	Estimation methods for AR model parameters	2
3.3	Non parametric spectrum estimation, Periodogram	2
3.4	Bartlett's method	1
3.5	Minimum variance estimation	2
4	**Module 4**	**9 hours**
4.1	Multi rate DSP - Decimators and Interpolators	2
4.2	Sampling rate conversion	1
4.3	multistage decimator & interpolator	2
4.4	Poly phase filters	2
4.5	Digital filter banks- two channel quadrature mirror filter banks	1
4.6	M-channel QMF bank	1
5	**Module 5**	**7 hours**
5.1	Application of DSP & Multi rate DSP	1
5.2	Application to Radar	1
5.3	Biomedical signal processing application	1
5.4	Application to image processing	1
5.5	Design of phase shifters	1
5.6	Use of DSP in speech processing	1
5.7	Multirate DSP Applications in sub-band coding	1

Reference Books

1. J.G.Proakis and D.G.Manolakis"Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007.

2. N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999.

3. Bruce W. Suter, "Multirate and Wavelet Signal Processing",1st Edition, Academic Press, 1997.

4. M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & SonsInc., 2002.

5. S.Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001.

6. Fredric J Harris, Multirate Signal Processing for Communication Systems, 1st Edition, Pearson Education, 2007.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE C007	ELECTRONIC PACKAGING	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: Electronic packaging has emerged as a competent field in the world of semiconductor manufacturing. This course intends to provide a basic knowledge of the technologies and processes required for the packaging of electronic products. The focus of the course will be on the packaging techniques and reliability studies of electronic packages.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	Select appropriate materials and techniques for the fabrication of an electronics package as per given application
CO 2	Understand various packaging techniques used in IC industry
CO 3	Understand the various steps in IC Assembly, Wafer level packaging and PCB manufacturing
CO 4	Analyze thermal management issues in IC packaging
CO 5	Analyze the failure mechanism in an electronics package
CO 6	Design a cooling technique for thermal management

Program outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3	-	-	-	-	-			1
CO 2	-	2	-	-	-	-		1	2
CO 3	-	-	1	2	1	1		2	1
CO 4	2	-	-	1	-	-		2	1
CO 5	-	3	2	-	2	-		1	2
CO 6	-	-	-	-	-	2		2	

Assessment Pattern

Bloom's Category	End Semester Examination (%)	Continuous Internal Evaluation (%)
Apply	50	50
Analyse	40	40
Evaluate	10	10
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No. : 10 marks

Test paper shall include a minimum of 80% of the syllabus

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M. TECH DEGREE EXAMINATION

Electronics & Communication Engineering (VLSI & EMBEDDED SYSTEMS)

24SJ1EEC007 Electronic Packaging

Max. Marks : 60 Duration: 2.5 Hours

PART A

Answer All Questions Each question carries 5 marks

1. List the key elements to determine what kind of IC package would best suit the needs of the application?
2. Describe RF packaging requirements.
3. Differentiate axial and radial leads in through hole technology
4. Illustrate the working of thermal vias as a cooling technique for electronic systems
5. Explain chemically induced failures in an electronic system

PART B

Answer Any Five Questions Each question carries 7 marks

6. Explain EMI issues in electronic packaging. Discuss any three methods to minimize EMI in electronic packages
7. Explain MCM physical design cycle
8. Explain 3 D packaging in detail
9. Illustrate how a suitable exit route be determined in a BGA layout
10. Suppose one need to package an application which should be sealed against atmosphere atmospheric, which sealing technique should be adopted. Illustrate the steps involved
11. Suggest a technique by which we can detect early failures in a batch of electronic devices
12. Suppose a sensor incorporating platinum is designed to monitor air quality. Since platinum is present, the sensor performance degrades in the presence of carbon monoxide. Devise an accelerated testing scheme so as to study the degradation caused to sensor by carbon monoxide.

Syllabus

MODULE 1:

Microsystems Packaging- Need of packaging, challenges in IC packaging, Role of packaging in computer industry, telecommunication industry, automotive industry, medical electronics and consumer electronics

Packaging Materials – electrical, thermal, mechanical and chemical properties, Future trends.

Fundamentals of electrical package design -anatomy of systems packaging, signaldistribution ,power distribution,Electromagnetic interference

MODULE 2:

Single Chip Packaging- Functions, Types, Fundamentals, characteristics, materials

Multi chip packaging- Multichip modules, functionality, advantages, multichip module technology comparisons, materials

RF packaging- Structure of RF systems, Fundamentals of RF packaging, Techniques for RF measurement, materials

MODULE 3:

IC Assembly- Need and Requirements of IC Assembly, wire bonding, Tape automated Bonding, Flip chip technology,materials

Wafer level packaging- Need and requirements for wafer level packaging,WLP technologies,Reliability aspects of WLP,Wafer level Burn in and Test,Materials

Printed Circuit Board –Board Assembly, Surface Mount Technology, Through-Hole Technology, Assembly Issues, Design challenges, materials

MODULE 4:

Thermal Management – Need for thermal management , Fundamentals of thermal management,Thermal management of IC and PCB packages, Cooling Requirements, Electronic cooling methods

Sealing and Encapsulation: Encapsulation requirements, Encapsulation materials, Encapsulation processes, Hermetic Sealing,materials

MODULE 5:

Design for Reliability – microsystems failure and failure mechanisms,thermo mechanically induced failures,Electrically induced failures,chemically induced failures-Accelrated Testing

Electrical Testing- Need for Electrical testing, system level electrical testing, interconncection tests,active circuit testing

Reference Books

1. Rao R. Tummala: Fundamentals of Microsystem Packaging McGraw Hill

2. Richard K. Ulrich &William D. Brown Advanced Electronic Packaging - 2nd Edition : IEEE Press
3. Charles A Harper, Electronic Packaging and Interconnection Handbook, McGraw hill, Fourth Edition

Course Plan

No	Topic	No. of Lectures
1	**Module 1**	
1.1	Basic concepts of systems packaging,	1
1.2	Role of packaging in computer industry, telecommunication industry, automotive industry, medical electronics and consumer electronics	1
1.3	Electrical and Thermal properties of packaging materials	1
1.4	Mechanical and Chemical properties of packaging materials	1
1.5	Power distribution and signal distribution aspects in an electrical package	1
1.6	Electromagnetic interference issues	1
2	**Module 2**	
2.1	Single Chip Packaging- Functions, Types, Fundamentals	1
2.2	Multi chip packaging modules, functionality, advantages	1
2.3	Multichip module technologies -programmable,non programmable	1
2.4	Non programmable MCM- MCM L, MCM C , MCM D	1
2.5	MCM C – LTCC and HTCC	1
2.6	MCM physical design cycle-partitioning, placement and routing	1
2.7	Fundamentals of RF packaging	1
3	**Module 3**	
3.1	IC assembly fundamentals	1
3.2	Wire bonding	1
3.3	Tape automated Bonding	1
3.4	Flip chip technology	1
3.5	Need and requirements for wafer level packaging	1
3.6	Wafer level chip scale packaging	1
3.7	Surface Mount Technology-BGA/PLCC/QFP	1
3.8	Through-Hole Technology	1
3.9	Printed Circuit Board Assembly Issues	1
4	**Module 4**	
4.1	Fundamentals and Need for thermal management	1
4.2	Thermal management of IC and PCB packages	1

4.3	Electronic cooling methods-Heat Pipes-Heat Sinks-Thermal vias	1
4.4	Design of heat sinks for packages	1
4.5	Design of Heat Pipes for cooling	1
4.6	Encapsulation process –Plastic, Non Hermetic	1
4.7	Materials used for encapsulation/sealing	1
4.8	Glass sealing	1
4.9	Hermetic Sealing	1
4.10	Electron Beam sealing	1
5	**Module 5**	
5.1	Thermo mechanically induced failures	1
5.2	Electrically induced failures	1
5.3	Chemically induced failures	1
5.4	System level electrical testing	1
5.5	Active circuit testing	1
5.6	Interconncection tests	1
5.7	Reliability aspects of WLP, Wafer level Burn in and Test	1
5.8	Accelerated Degradation Modeling, Environmental Stress Screening	1
	Total	40

CODE 24SJ1E EC010	COURSE NAME ADVANCED COMPUTER ARCHITECTURE	CATEGORY	L	T	P	CREDIT
		PE 1	3	0	0	3

Preamble: Nil

Course Outcomes:

CO 1	To Realize Data Path Unit (DPU) and Control Unit (CU)
CO 2	To Analyze the Performance of Multi-Core Architectures
CO 3	To Demonstrate OpenCL Programs for real time applications
CO 4	To Implement Kernels for Heterogeneous Architectures in OpenCL
CO 5	To List and Describe the Challenges in Advanced Parallel Processing Architectures

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2
CO1	3	1	3		3	2		2	
CO2	3	2	3	3	3	3	1	2	1
CO3	3	2	3	3	3	3	1	2	1
CO4	3	2	2	2	2	3		2	2
CO5	2		1		1	1		2	2

Assessment Pattern:

Bloom's Category	CIE	End Semester Examination
Apply	10	20
Analyse	10	20
Evaluate	20	20
Create		

Mark distribution:

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 Hours

Continuous Internal Evaluation Pattern:

Evaluation shall only be based on application, analysis or design-based questions

(for both internal and end semester examinations).

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course based task/Seminar/Data collection and interpretation: 15 marksTest paper, 1 no.: 10 marks
Test paper shall include minimum 80% of the syllabus.

End Semester Examination: 60 marks

The end semester examination will be conducted by the Institute . There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 5 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module ofwhich student shall answer any five. Each question can carry 7 marks. Total duration of the examination will be 150 minutes.

Syllabus

Module I (8)

Processor Design: CPU Design– CPU Organization – Data Path Design: Fixed Point Booth‟s Multiplier, Restoring Division Unit and Non-Restoring Division Unit. Memory Hierarchy – Virtual Memory – Cache Memory Control Unit Design – Hardwired Control Unit Design of Basic CPU. Case Studies:Verilog HDL Implementation of Booth‟s Multiplication, Restoring and Non Restoring Division and Hardwired Control Unit Realization of Basic CPU

Module II (8)

Multi Core Architectures:

RISC, CISC, Flynn‟s Classification, Instruction Level Parallelism: Super Scalar, VLIW and EPIC architectures. Scalable, Multithreaded and Dataflow Architectures: Principles of Multithreading,Fine-Grain Multithreading, Scalable and Multithreaded Architectures and Dataflow and Hybrid Architectures. Case Studies:Threads and OpenMP

Module III (8)

Accelerated Architectures: GPU: nVidia and AMD Architecture – GPU memory and Scheduling, Parallel Programming Development and Environment: MPI – CUDA – OpenCL: Introduction, Platform and Devices, Execution Environment and Memory Model

Case Studies: OpenCL programming

Module IV (7)

Low Power Architectures: System on Chip Architectures – Raspberry-Pi, nVidia SoC – Basics of Kernels: Kernels, Work-items, Work-groups and Execution Domain, OpenCL Synchronization

Case Studies: Programming on Raspberry Pi.

Module V (8)

Advances in Parallel Processor Architectures:

Hybrid Architectures– Issues and Challenges in Heterogeneous Computing, Schedulers, Process Synchronization and Programming

Virtualization– Processor and Memory

Case Studies: Hybrid Programming using CPU and GPU

Text Books:

1 Hayes John P, "Computer Architecture and organization," 3 rd edition, McGraw Hill Education,1998.

2 William Stallings, "Computer Organization and Architecture: Designing for Performance", 8 thedition, PHI, 2007.

3 Hwang and Naresh Jotwani, "Advanced Computer Architecture: Parallelism, Scalability andProgrammability," McGraw Hill Education, 2017.

4 Benedict Gaster, Lee Howes, David R. Kaeli, Perhaad Mistry and Dana Schaa, "HeterogeneousComputing with OpenCL," Morgan Kaufmann Publications, 2011.

SEMESTER I

PROGRAM ELECTIVE II

SLOT	SL NO	COURSE CODE	COURSE NAME	L-T-P	HOURS	CREDIT
E	1	24SJ1EEC039	VLSI SIGNAL PROCESSING	3-0-0	3	3
	2	24SJ1EEC101	ADVANCED DIGITAL SYSTEM DESIGN	3-0-0	3	3
	3	24SJ1EEC040	DIGITAL DESIGN PRINCIPLES AND APPLICATIONS	3-0-0	3	3
	4	24SJ1EEC041	FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG	3-0-0	3	3
	5	24SJ1EEC042	ASIC DESIGN	3-0-0	3	3
	6	24SJ1EEC043	EMBEDDED OPERATING SYSTEM	3-0-0	3	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EEC039	VLSI SIGNAL PROCESSING	PROGRAM ELECTIVE 2	3	0	0	3

Preamble: The course aims at presenting various signal processing algorithms optimised for VLSI design. Also, it helps in performing pipelining, parallel processing, retiming, fording and unfolding for enhancing the performance of VLSI architectures.

Course Outcomes:

After the completion of the course the student will be able to:

CO 1	Analyse circuit graphs for iteration bound and loop bound
CO 2	Design pipelined and parallel processed FIR filters
CO 3	Perform retiming to minimize clock period for VLSI design
CO 4	Design unfolding and folding transformations
CO 5	Understand systolic architectures and fast convolution

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	1		2	2				2	1
CO 2	1		2		1		1	1	2
CO 3	1		2	2		2		2	2
CO 4	1		2				2	2	1
CO 5	1		2					2	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	15
Analyse	15
Evaluate	30
Create	-

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation(CIE) Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M. TECH DEGREE EXAMINATION

Electronics & Communication Engineering (EC5)

(Advanced Electronics and Communication Engineering)

Course Code: 24SJ1EEC039 Course

Name: VLSI Signal Processing

(Model Question Paper)

Max. Marks : 60 Duration: 2 Hrs 30 Minutes

PART A

(5X5=25marks)

Answer All Questions, each carries 5 marks

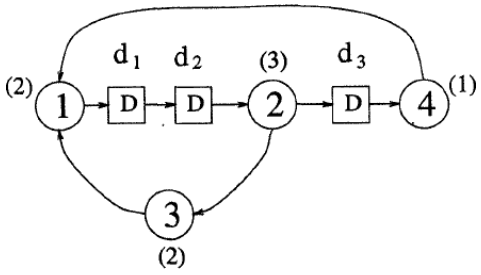
1. Explain how power consumption can be reduced by parallel processing?
2. Give quantitative description of retiming.
3. Prove that unfolding preserves number of delays in a DFG.
4. What are the applications of folding transformation?.
5. What you mean by a systolic array?

PART B

(5X7=35 marks)

Answer any 5. Each question carries 7 marks

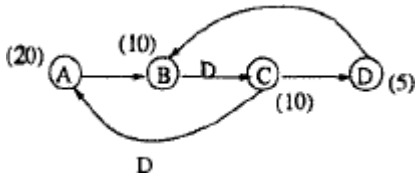
6. Compute the iteration bound of the DFG shown using MCM algorithm. Assume computation times of nodes are given in parentheses.



7. Explain the steps involved in computing iteration bound of a multi rate DFG.

8. Consider a 3 tap FIR filter $(n) = ax(n) + bx(n-1) + cx(n-2)$. Get a 3-parallel architecture for this filter.

9. Consider the DFG with number at each node denoting the execution time. What is the fundamental limit on the system described by this DFG. Retime this DFG to minimize the clock period.



10. Explain life time analysis with an example involving 3 variables a, b, c, live during $n \in \{1,2,3,4\}$, $n \in \{2,3,4,5,6,7\}$, $n \in \{5,6,7\}$, respectively.

11. Explain the design B_1 for FIR systolic arrays.
12. Construct a 2 × 2 Cook-Toom convolution algorithm using $\beta = 0, \pm 1$.

Syllabus

Module-1-Iteration bound Representation of DSP algorithms-Block diagram-SFG, DFG, Dependence graph, Critical path, loop bound, iteration bound, Iteration Bound Algorithm-Longest path matrix algorithm, Iteration Bound for multi-rate data flow graphs-simple examples.
Module-2-Pipelining and Parallel Processing Pipelining of FIR digital filters, fine grain pipelining, Parallel Processing FIR filter design, Pipelining and parallel processing for low power
Module-3-Retiming Introduction, definitions and properties, Retiming techniques- cutset retiming and pipelining, Shortest path algorithms-Bellman Ford and Floyd-Warshall Algorithms, Solving system of inequalities, retiming for clock period minimisation
Module-4-Unfolding and folding Unfolding- unfolding algorithm, properties, critical path unfolding and retiming, unfolding for sample period reduction, Folding- Introduction, folding transformation, register minimization- lifetime analysis and data allocation using forward-backward register allocation
Module-5- Systolic architecture and fast convolution Systolic Design Methodologies, FIR systolic array, matrix-matrix multiplication and 2-D systolic array design, Fast convolution: Cook Toom, Winograd algorithms, Iterated convolution

Reference Books

1. K. K. Parhi, "VLSI Digital Signal Processing", Wiley India, 2008

2. P. Pirsch, "Architecture for Digital Signal Processing", Wiley, 2011.

3. M. A. Bayoumi, “VLSI Design Methodologies for DSP Architecture”, Kluwer Academic, 1993.

Course Plan

No	Topic	No. of lecture hours
1	**Iteration bound**	
1.1	Representation of DSP algorithms-Block diagram-SFG, DFG, Dependence graph	2
1.2	Critical path, loop bound, iteration bound	2
1.3	Iteration Bound Algorithm-Longest path matrix algorithm, Iteration Bound for multi-rate data flow graphs-simple examples.	4
2	**Pipelining and Parallel Processing**	
2.1	Pipelining of FIR digital filters, fine grain pipelining	2
2.2	Parallel Processing FIR filter design	2
2.3	Pipelining and parallel processing for low power	4
3	**Retiming**	
3.1	Introduction, definitions and properties, Retiming techniques-cutset retiming and pipelining	2
3.2	Shortest path algorithms-Bellman Ford and Floyd-Warshall Algorithms, Solving system of inequalities	4
3.3	retiming for clock period minimisation	2
4	**Unfolding and Folding**	
4.1	Unfolding- unfolding algorithm, properties, critical path unfolding and retiming, unfolding for sample period reduction	4
4.2	Folding- Introduction, folding transformation	2
4.3	register minimization-lifetime analysis and data allocation using forward-backward register allocation	2
5	**Systolic architecture and fast convolution**	
5.1	Systolic Design Methodologies, FIR systolic array	3
5.2	matrix-matrix multiplication and 2-D systolic array design	2
5.3	Fast convolution: Cook Toom, Winograd algorithms, Iterated convolution	3

CODE	COURSE	CATEGORY	L	T	P	CREDIT
24SJ1EE C035	DESIGN WITH ADVANCED MICROCONTROLLER	PROGRAM ELECTIVE I	3	0	0	3

Preamble: The purpose of this course is to provide a solid foundation that furnishes the learner with in-depth knowledge of advanced microcontrollers. The syllabus covers two advanced microcontrollers. One is of ARM core and the other is with DSP core. This course covers architecture, programming, tools for development, testing and debugging and application notes. This course helps the learner to design an embedded system as per the requirement and implement with a professional grade.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Study ARM Processor architecture and programming model. **(Cognitive Knowledge Level: Analyse)**
CO 2	Analyze a problem statement and design a solution based on ARM processor-based embedded systems **(Cognitive Knowledge Level: Evaluate)**
CO 3	Study DSP Processor architecture and programming model. **(Cognitive Knowledge Level: Analyse)**
CO 4	Analyze a problem statement and design a solution based on DSP processor-based embedded systems **(Cognitive Knowledge Level: Evaluate)**
CO 5	Identify a practical problem and develop a solution based on the appropriate processor and create an application note for the prescribed solution. **(Cognitive Knowledge Level: Create)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards

PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1			1			1		2	2
CO 2	2		2	3	3	1		1	1
CO 3			1			1		1	
CO 4	2		2	3	3	1		1	
CO 5		1	2	2	3	2	3	1	1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination (%)
Apply	30	40
Analyse	30	35
Evaluate	25	25
Create	15	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No. : 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ1EEC035

Course Name: Design with Advanced Microcontroller

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. What are the functions of the supervisory mode of operation in ARM processor?
2. Explain a generic program status register used in ARM with a detailed description of all fields
3. Write the number 2005 in 32-bit binary, binary coded decimal, ASCII and single precision floating point notation.
4. What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with diagram.
5. Find the impulse response of an FIR filter with N=11,a sampling frequency of 10khz,and a cutoff frequency fc=1khz.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Which window function can be used for better selectivity? Compare it with other window functions.

7. Develop a C Program for the Band Stop filter with an enter frequency of 2700Hz. Select the number of coefficients appropriately.
8. Find the impulse response of an FIR filter with N=11,a sampling frequency of 10khz,and a cutoff frequency fc=1khz.
9. Explain the most widely used industrial serial communication protocol available in LPC1769 microcontroller.
10. In ARM processor (LPC1769) show the clock generation for different modules from the available oscillators.
11. Estimate proportion of the number of test vectors required to test an ARM core via the JTAG and AMBA interface.
12. Describe and differentiate between production VLSI testing, printed circuit board testing and system debugging, and describe how a JTAG test port may be used to address each of these.

(5x7=35 Marks)

Syllabus

Module 1 (ARM Processor)

ARM Processor Architecture: Functional block Diagram, RISC advantage, Register set, Pipeline, Exceptions & Interrupts, Memory mapping control. ARM Peripherals access: Crystal oscillator, PLL, reset and wakeup timer, Timers, Event counters, Interrupt, ADC, DAC, PWM. Communication protocols: UART, SPI, I2C, CAN, USB, Ethernet.

Module 2 (ARM processor tools and programming)

Architectural support for high level languages-Data types, Floating point data types, Conditional statements, Loops, Use of memory, Run-time environment, Programmer`s model, Development tools. Architectural support for system development- ARM memory interface, AMBA, ARM reference peripheral specifications, H/W system prototyping tools, ARM emulator, JTAG, ARM debug architecture, Embedded trace, signal processing support.

Module 3 (DSP Processor)

Digital Signal Processors- Functional overview, Memory Mapping, fetch and execute, pipelining, Linear and circular addressing modes, Memory bus, peripheral bus, Oscillator, PLL and clocking mechanisms, interrupts. DSP Peripherals: Direct Memory Access (DMA), CPU-Timers, PWM modules, enhanced capture modules, QEP modules, analog-to-digital converter (ADC) module, controller area network modules, serial communications interface modules, serial peripheral interface (SPI) module, Inter-integrated circuit module (I2C), Digital I/O and shared pin functions.

Module 4 (DSP operations)

Filter design in DSP processor: Introduction to z-transform, Mapping from s-Plane to z- Plane, Difference Equations, Discrete Signals, Finite Impulse Response (FIR) Filters, FIR Implementation Using Fourier Series, Lowpass FIR Filter, Window Functions, Computer-Aided Approximation, Programming Examples Using C and ASM code, FIR Filter Implementation: Band-stop and Band-pass.

Module 5 (Case Study)

Design of real-time clock and stop watch using ARM processor. Design a practical filter using the DSP processor, and analyse the effectiveness of DSP application by using specific processor.

Reference Books

1. Rulph Chassaing, "DSP Applications Using C and the TMS320C6x DSK", RulphChassaing, John Wiley & Sons Inc, 2002.
2. Robert Oshana, "DSP Software Development Techniques for Embedded and Real-Time Systems", Newnes, 2006.
3. Steve Furber, "ARM System-on-chip architecture", Pearson Education.
4. Wayne Wolf, "Computers as Components-principles of Embedded computer system design", Elseveir.
5. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide", Elseveir.
6. David E. Simon, "An Embedded Software Primer", Pearson Education.
7. TMS320F28335 datasheet.
8. LPC1769 datasheet.

Syllabus and Course Plan

No	Topic	No. of Lectures
1	**ARM Processor**	**8 hours**
1.1	Functional block Diagram, RISC advantage	1
1.2	Register set, Pipeline, Exceptions & Interrupts	1
1.3	ARM Peripherals access: Crystal oscillator, PLL, reset and wakeup timer, Timers, Event counters, Interrupt	1
1.4	ADC, DAC, PWM	1
1.5	Communication protocols: UART	1
1.6	SPI, I2C	1
1.7	CAN, USB	1
1.8	Ethernet	1
2	**ARM processor tools and programming**	**8 hours**

2.1	Architectural support for high level languages-Data types, Floating point data types, Conditional statements, Loops, Use of memory	1
2.2	Programmer`s model	1
2.3	Development tools	1
2.4	Architectural support for system development- ARM memory interface, AMBA, ARM reference peripheral specifications	1
2.5	H/W system prototyping tools	1
2.6	ARM emulator	1
2.7	JTAG, ARM debug architecture	1
2.8	Embedded trace, signal processing support	1
3	**DSP Processor**	**8 hours**
3.1	TMS320F28335 digital signal Processor, functional overview	1
3.2	Memory Mapping, fetch and execute, pipelining, Linear and circular addressing modes	1
3.3	Memory bus, a peripheral bus	1
3.4	Oscillator, PLL and clocking mechanisms, Interrupts	1
3.5	DSP Peripherals: Direct Memory Access (DMA), CPU-Timers, PWM modules, enhanced capture modules, QEP modules	1
3.6	analog-to-digital converter (ADC) module	1
3.7	Controller area network modules	1
3.8	serial communications interface modules, serial peripheral interface (SPI) module, Inter-integrated circuit module (I2C)	1
4	**DSP operations**	**8 hours**
4.1	Filter design in DSP processor: Introduction to z-transform, Mapping from s-Plane to z-Plane	1
4.2	Difference Equations, Discrete Signals	1
4.3	Finite Impulse Response (FIR) Filters	1
4.4	FIR Implementation Using Fourier Series, Lowpass FIR Filter	1
4.5	Synchronization: The Basics	1
4.6	Window Functions	1
4.7	Computer-Aided Approximation, Programming Examples Using C and ASM code	1
4.8	FIR Filter Implementation: Band-stop and Band-pass	1
5	**Case study**	**8 hours**
5.1	Programming basics of ARM Processor	1
5.2	Programming tools of ARM processor	1
5.3	Perform the software design of a blinky program with ARM.	1
5.4	Design the Clock and stopwatch using ARM and test on any Development board.	1
5.5	Programming basics of DSP Processor	1
5.6	Programming tools of DSP processor	1
5.7	Perform the software design of a blinky program with DSP.	1
5.8	Design a filter with the given parameters using DSP and test on any Development board.	1
	Total	**40**

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE C040	DIGITAL DESIGN PRINCIPLES AND APPLICATIONS	PROGRAM ELECTIVE II	3	0	0	3

Preamble:

· To introduce methods to analyze and design synchronous and asynchronous sequential circuits
· To introduce the architectures of programmable devices
· To introduce design and implementation of digital circuits using programming tools

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyse and design synchronous and asynchronous sequential digital circuits.
CO 2	Design and use programming tools for implementing digital circuits of industry standards.
CO 3	Analyse different methods for fault identification and fault diagnosis in digital circuit.
CO 4	Examine the basic architecture and other features of different FPGAs.
CO 5	Understand modelling and verification with hardware description languages

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2							2	
CO 2	2		2		2	2	2	2	2
CO 3	2				2			1	2
CO 4			2				2	1	2
CO 5	2		2		2				1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation	End Semester Examination
Apply	40 %	40 %
Analyse	35 %	35 %
Evaluate	25 %	25 %
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No.: 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

First Semester M.Tech Degree Examination

December 20xx ELECTRONICS AND COMMUNICATION ENGINEERING (VLSI & EMBEDDED SYSTEMS)

Time: 2.5 hrs. Max. Marks: 60

DIGITAL DESIGN PRINCIPLES AND APPLICATION

PART – A 25 Marks

1) Define Mealy and Moore model.

2) Write about static and dynamic hazards in combinational circuit.

3) Differentiate between truth table and D algorithm singular cover.

4) How does architecture of PAL differ from that of a PAL

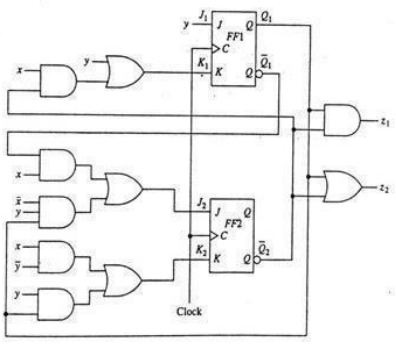
5) Write VHDL code for half adder.

PART – B 35 Marks

6)

A. Design a synchronous sequential circuit for the count sequence 6- 4-3-7-1-6-4- 3-7-1... (3 marks)

B. For the clocked synchronous sequential circuit shown in figure construct transition table (4 marks)



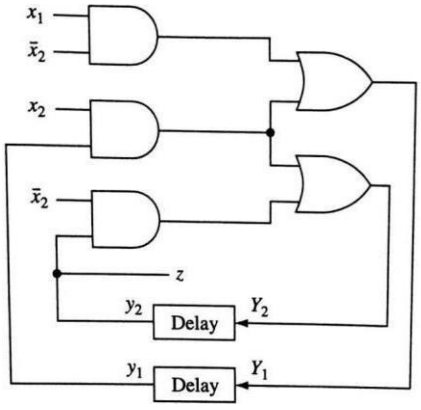
7. Design a coin-operated vending machine control unit which dispenses candy under the following conditions: **(7 marks)**

- The machine accepts 5-cent coin and 10-cent coin only.
- It takes 10 cents for a piece of candy to be released from the machine.
- If 15 cents is deposited, the machine will not return the change, but it will credit thebuyer with 5 cents and wait for the buyer to make a second purchase.

8. Write about races in asynchronous sequential circuit, and its elimination techniques with examples. (7marks)

9. Analyze the asynchronous sequential circuit shown in figure by forming the excitation table /transition table, state table, flow table and flow diagram. The network operates in fundamental mode with restriction that only one input variable can change at a time.

(7marks)



10. briefly write about the following terms with suitable examples (7marks)

a. path sensitization method

b. Boolean difference method.

11. Design a seven-segment display unit using suitable programmable logic device (7marks)

12. Design 4:1 multiplexer using behavioural modelling (7 marks)

Syllabus

MODULE I SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits and modelling - State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM

MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronouscircuits – designing vending machine controller

MODULE III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Folded PLA‘s -Fault in PLA – Weinberger arrays – gate matrices – Test generation-DFT schemes – Built in self-test

MODULE IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD.Capacitive parasitic - Capacitance and performance in CMOS – driving large capacitance – Resistive parasitic – Resistance and performance in CMOS. FPGA – Xilinx FPGA-Xilinx 4000 Programmable logic array designs – Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture.

MODULE V SYSTEM DESIGN USING VERILOG

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators for Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

Syllabus and Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
	Digital Design Principles and Application	
1	**Module 1**	

1.1	Analysis of clocked synchronous sequential circuits and modelling.	1
1.2	State diagram, state table, state table assignment and reduction-	2
1.3	Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM	2
2	**Module 2**	
2	Analysis of asynchronous sequential circuit flow table reduction	2
2.1	races-state assignment-transition table and problems in transition table	2
2.2	Design of asynchronous sequential circuit	2
2.3	Static, dynamic and essential hazards	2
2.4	Data synchronizers – mixed operating mode asynchronous circuits	1
2.5	Designing vending machine controller	1
3	**Module 3**	
3.1	Fault table method-path sensitization method	1
3.2	Boolean difference method-D algorithm	2
3.3	Tolerance techniques	1
3.4	The compact algorithm	1
3.5	Fault in PLA Folded PLA	2
3.6	Test generation-DFT schemes	1
3.7	Built in self-test	1
4	**Module 4**	
4.1	Designing a synchronous sequential circuit using PLA/PAL –	1
4.2	Realization of finite state machine using PLD	1
4.3	Capacitive parasitic - Capacitance and performance in CMOS – driving large capacitance	2
4.4	Resistive parasitic – Resistance and performance in CMOS.	1
	FPGA – Xilinx FPGA-Xilinx 4000 Programmable logic array designs	1
4.5	Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture –	1
4.6	ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture.	1

5	**Module 5**	
5.1	Hardware Modelling with Verilog HDL	1
5.2	Logic System, Data Types and Operators for Modelling in Verilog HDL	1
5.3	Behavioural Descriptions in Verilog HDL	1
5.4	HDL Based Synthesis – Synthesis of Finite State Machines	2
5.5	structural modelling – compilation and simulation of Verilog code	
5.6	Test bench - Realization of combinational and sequential circuits using Verilog	1
5.7	Registers – counters – sequential machine	1
5.8	serial adder – Multiplier- Divider – Design of simple microprocessor	1

Reference Books

1. Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004

2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999

3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999

4. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001

5. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S

6. Parag K.Lala "Digital system Design using PLD" B S Publications,2003

7. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EE C041	FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG	PROGRAM ELECTIVE 2	3	0	0	3

Preamble: The purpose of this course is to provide a detailed explanation of Hardware verification language features and concepts used in the industry to verify the functional features of the digital system design, it speed up the verification process of the learner. Learner can construct a flexible and reliable verification environment from scratch. These environment components can be re-used across multiple projects. At the end of the course learner can build Bus Functional Models(BFMs)and evaluate the performance of the DUT based on Universal Verification Methodology (UVM)

Course Outcomes: After the completion of the course the student will be able to

CO #	CO
CO 1	Understand the basics of Hardware verification and important features of Systemverilog for Hardware verification
CO 2	Able to design the Race free TestBench for Design Under Test(DUT)
CO 3	Analyze the performance evaluation of the design by using performance evaluation metrics
CO 4	Design of Verification IP(VIP) using Universal Verification Methodology(UVM)
CO 5	Design of Bus Functional Models(BFMs) for different applications

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.

PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2					1		2	
CO 2	2	2	2		2	1	2	2	2
CO 3	2				2			1	2
CO 4			2				2	1	2
CO 5	2		2		2				1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination (%)
Apply	40	40
Analyse	35	35
Evaluate	25	25
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Syllabus

Module 1

Basics of Verification: Verification Methodologies, Difference between verification & testing, Importance of hardware verification languages and methodologies.

Introduction to SystemVerilog: SystemVerilog data types, 4-state & 2-state types, typedefs, enum, struct data type.Packages, strings, static and dynamic type casting.

Module 2

System Verilog operators and functions: loops in system Verilog, always blocks, tasks and functions case if and if-else statements, time scale. Structures, Arrays, Semaphores and Mailboxes: Structs and its assignments, packed and unpacked arrays, associative arrays and methods, queues, semaphores and mailboxes.

Class and Extensions : System Verilog class basics, class declaration, class members and methods, class handles, 'super' and 'this' keywords, user defined constructors, class extension/ inheritance, new constructors, extending class methods, Virtual class, polymorphism using virtual methods.

Module 3

Connecting the Testbench and Design: Test benches, Layered Organization of Test benches , Separating the Test bench and Design, Interface overview.

Program block: Fundamental test bench construction, program blocks, program block interaction with modules. **Clocking:** Clocking blocks, clocking skews, fork-join processes.

Module 4

Constrained Randomization: Random variables & built in-randomization methods, random sequence & examples, Randomization constraints, constraint distribution and set membership. **Coverage Metrics**: Covergroups, coverpoints, coverpoint bins and labels, cross coverage.

Module 5

UVM based Verification: UVM Environment components: Transaction, Sequence, Configuration Object, Driver, Sequencer, Monitor, Coverage collector Agent.

UVM Test Bench Architecture: Top, Test, Environment Agent & DUT Design of Bus Functional Models(BFMs)

Course Plan		
Module	**Contents**	**Hours Allotted**
I	**Basics of Verification:** Verification Methodologies, Difference between verification & testing, Importance of hardware verification languages and methodologies. **Introduction to SystemVerilog:**SystemVerilog data types, 4-state & 2-state types, typedefs, enum, struct data type.Packages, strings, static and dynamic type casting.	8
II	**SystemVerilog operators and functions**: loops in system Verilog,always blocks, tasks and functions case if and if-else statements, time scale. Structures, Arrays, Semaphores and Mailboxes:Structs and its assignments, packed and unpacked arrays, associative arrays and methods, queues, semaphores and mailboxes. **Class and Extensions :**SystemVerilog class basics, class declaration,class members and methods, class handles, 'super' and 'this' keywords,user defined constructors, class extension/inheritance, new constructors, extending class methods, Virtual class, polymorphism using virtual methods.	8
III	**Connecting the Testbench and Design:** Test benches, Layered Organization of Test benches , Separating the Testbench and Design, Interface overview. **Program block:** Fundamental testbench construction, program blocks, program block interaction with modules. **Clocking:** Clocking blocks, clocking skews, fork-join processes.	8
IV	**Constrained Randomization:** Random variables & built in-randomization methods, random sequence & examples, Randomization constraints, constraint distribution and set membership. **Coverage Metrics**: Covergroups, coverpoints, coverpoint bins and labels, cross coverage.	8
V	**UVM based Verification**: UVM Environment components: Transaction,Sequence,ConfigurationObject, Driver, Sequencer, Monitor, Coverage collector Agent. **UVM TestBench Architecture**:Top,Test,Environment Agent & DUT Design of Bus Functional Models(BFMs)	8

Reference Books

1. Chris Spear, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Springer-Verlag New York, Inc. Secaucus, NJ,USA, 2006
2. Mintz, Mike, Ekendahl, Robert, Hardware Verification with System Verilog, XXII, 314 p., Springer, ISBN: 978-0-387-71738-8 2007
3. Janick Bergeron Writing Testbenches using System Verilog, Springer
4. Stuart Sutherl, Simon Davidmann and Peter Flake (Author) System Verilog For Design: A Guide to Using SystemVerilog for Hardware Design and Modeling Kluwer Academic Publisher
5. http://www.asic-world.com/systemverilog/tutorial.html
6. http://www.vhdl.org/sv/SystemVerilog_3.1a.pdf
7. http://www.systemverilog.in/

Model Question Paper

QP CODE: **PAGES: 3**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ1EEC041 Course Name: Functional Verification with SystemVerilog

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Differentiate between **Verification and Validation** in SystemVerilog?
2. Differentiate between **Function and Task** in SystemVerilog? Explain with an example?
3. Justify how **Program block** is used to avoid **Race condition** in design of Test bench?
4. Explain the importance of weighted distribution in SystemVerilog? Explian with an example?
5. Explain Synchronization mechanism between Sequencer and Driver in UVM methodology?

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Explain the verification flow of the Digital System Design?
7. Explain Procedural Assignment statements in SystemVerilog? Predict the **simulator output** of the below given program?

```
module block();
integer a,b,c;
initial  begin
$monitor ("[%0t] a=%0d b =%0d c= %0d ", $time, a, b, c);
a=10;b=5;c=15;
#1  a=b+c;
#2  b=a+5;
```

```
#3  c=a-b;
end

Endmodule
```

8. Design a Module and Test bench for 4:1 Multiplexer in SystemVerilog?

9. Explain how the **fork and Join** process works in SystemVerilog**?** Predict the **simulator output** of the below given program?

```
program main;
initial begin
$display(" First fork time = %d",$time );
fork
begin  #10;
$display("time1 = %d",$time);
end
begin
#(5);
$display("time2 = %d",$time);
#(2);
$display("time3 = %d",$time);
end
join
$display(" time = %d Outside the main fork ",$time );
end
endprogram
```


10. What are the performance evaluation metrics in SystemVerilog? Explian different types of constructs used for functional coverage implementation in systemverilog?

11. Design of SPI Master slave controller Verification IP (VIP) using UVM methodology in SystemVerilog ?

12. Design of Bus Functional Model(BFM) for Advanced Peripheral Bus (APB) protocol ?

(5x7=35 Marks)

Course Plan

No	Topic	No. of Lectures
1	**Basics of Verification**	**8 hours**
1.1	Verification process flow diagram	1
1.2	Different verification methods	1
1.3	Difference between verification & testing	1
1.4	Importance of hardware verification languages	1
1.5	SystemVerilog supporting data types	1
1.6	Difference between 4-state & 2-state data types	1
1.7	Typedefs, enum, struct data type	1
1.8	Static and Dynamic data type casting.	1
2	**SystemVerilog operators and functions &class constructor**	**8 hours**
2.1	Types of loops in system Verilog,always blocks	2
2.2	Tasks and functions case if and if-else statements	1
2.3	Structures, Arrays, Semaphores and Mailboxes	1
2.4	Packed and unpacked arrays, associative arrays	1
2.5	SystemVerilog class basics	
2.6	Class declaration,class members and methods	1
2.7	Class declaration,class members and methods	1
2.8	Class extension/inheritance, new constructors, extending class methods	1
3	**Testbench,Program block&clocking block**	**8 hours**
3.1	Layered Organization of Test benches	2
3.2	Separating the Testbench and Design,	1
3.3	Interface overview,modport	1
3.4	Program blocks	2
3.5	Clocking blocks, Clocking skews,	1
3.6	Fork-join processes	1
4	**Constrained Randomization**	**8 hours**
4.1	Constrained Randomization,weighted distrubution	2
4.2	Random variables & built in-randomization methods	1
4.3	Random sequence & examples	1
4.4	Randomization constraints, constraint distribution	1
4.5	Set membership	1
4.6	Covergroups, Coverpoints, coverpoint & bins	2

5	**UVM based Verification**	**8 hours**
5.1	UVM based verification overview, Transaction,Sequence	2
5.2	Configuration Object,Driver	1
5.3	Sequencer,Monitor& Agent.	1
5.4	Top &Test	1
5.5	Environment Agent & DUT	1
5.6	Design of Bus Functional Models(BFMs)	2

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ1EEC042	ASIC DESIGN	PROGRAM ELECTIVE 2	3	0	0	3

Preamble: The purpose of this course is to provide fundamentals in ASIC Design, Architecture and programmability. The Course describes the learning level of ASICs from the level of cell design, device simulation and synthesis. The concept of Logic design helps tounder the subject in micro level.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Study the fundamentals of the ASIC. **(Cognitive Knowledge Level: Analyse)**
CO 2	Apply CMOS Designs based on rules and different logic cell element designs **(Cognitive Knowledge Level: Apply)**
CO 3	Evaluate the cell designs and architectures. **(Cognitive Knowledge Level: Evaluate)**
CO 4	Apply the programmable ASICs with solutions **(Cognitive Knowledge Level: Apply)**
CO 5	Evaluate the devices and synthesis followed. **(Cognitive Knowledge Level: Evaluate)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards

PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2	2						2	
CO 2	2		2		2	2	2	2	2
CO 3	2	2			2			1	1
CO 4			2				2	2	2
CO 5	2		2		2			1	1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination (%)
Apply	40	40
Analyse	35	35
Evaluate	25	25
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE: **PAGES:2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code:

24SJ1EEC042

Course Name: ASIC Design

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. What are the types of ASICs?
2. Evaluate the channelled Gate Array and Channelless Array.
3. Sketch the CMOS and mention the rules.
4. What is the role adders and multipliers.
5. Give a detail account on the Library architecture used in the design.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Evaluate the architecture advantages of Xilinx LCA.
7. Evaluate the architecture in Altera Flex, Altera Max.
8. Find the AC Output, DC Input, AC Input, Clock Input with respect to the programmability of ASIC.
9. Explain the most Actel ACT, Xilnx LCA and analyse the features.
10. Analyse the usage of Altera Max 5000 and 7000 with examples.
11. Write a VHDL programme to control the digital input output system
12. Why Xilinix EPLD is having more superiority than other hardware's in terms of effciiency. Give the facts?

(5x7=35 Marks)

Syllabus

Module-1 (ASIC Fundamentals)

Introduction to ASICs-Types of ASICs: Full Custom ASICs, , Standard Cell based ASICs, Gate Array based ASICs, Channeled Gate Array, Channelless Gate Array, Structured Gate Array, Programmable Logic Devices, Field Programmable Gate Arrays. Design Flow, ASIC Cell Libraries.

Module-2 (CMOS Designs)

CMOS Transistors-CMOS Process, CMOS Design Rules, Combinational Logic Cells, Sequential logic Cells, Latch, Flip-flops, Clocked inverter. Data path logic Cells: Data path elements, Adders, Multipliers, I/O Cells, Cell Compilers.

Module-3 (Cell Designs and Architecture)

Transistors as Resistors-Transistors parasitic capacitance: Junction capacitance, Overlap capacitance, Gate Capacitance, Slew Rate, Logical Effort: Predicting Delay, Logical Area and logical efficiency, Logical path, Multistage cells, Optimum delay, Optimum number of stages, Library Cell Design, Library Architecture, Gate Array Design, Standard Cell Design, Data Path Cell design.

Module-4 (Programmability)

Programmable ASICs- Antifuse, Static Ram, EPROM and EEPROM Technology, Practical issues, Specifications, Programmable ASIC logic cells: Actel ACT , Xilinx LCA, Altera Flex, Altera Max, Programmable ASIC I/O cells: DC output, AC Output, DC Input, AC Input, Clock Input, Power Input, Xilinx I/O block.

Module-5 (Devices and Synthesis)

Programmable ASIC Interconnect-Actel ACT, Xilnx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera Flex, VHDL, Verilog HDL, Logic Synthesis.

Reference Books

1. "Application-Specific Integrated Circuits", ~~Michael John Sebastian Smith~~ June 1997.

2. "Application-Specific Integrated Circuits", ~~Michael John Sebastian Smith~~, January 2002

3.” Application Specific Integrated Circuit (ASIC) Technology”, Norman G. Einspruch and Jeffrey L. Hilbert Published 1991

4. “High Performance ASIC Design”, Razak Hossain, 2009

Syllabus and Course Plan

No	Topic	No. of Lectures
1	**ASIC Fundamentals-8 hours**.	
1.1	Introduction to ASICs-Types of ASICs: Full Custom ASICs,	1
1.2	Standard Cell based ASICs, Gate Array based ASICs,	1
1.3	Channelled Gate Array	1
1.4	Channelless Gate Array	1
1.5	Structured Gate Array	1
1.6	Programmable Logic Devices	1
1.7	Field Programmable Gate Arrays	1
1.8	Design Flow, ASIC Cell Libraries	1
2	**CMOS Designs-8 hours**	
2.1	CMOS Transistors-CMOS Process,	1
2.2	CMOS Design Rules	1
2.3	Combinational Logic Cells	1
2.4	Sequential logic Cells, Latch	1
2.5	Flip-flops, Clocked inverter.	1
2.6	Data path logic Cells: Data path elements,	1
2.7	Adders, Multipliers	1
2.8	I/O Cells, Cell Compilers	1
3	**Cell Designs and Architecture- 8 hours**	
3.1	Transistors as Resistors	1
3.2	Transistors parasitic capacitance: Junction capacitance,	1
3.3	Overlap capacitance, Gate Capacitance	1
3.4	Slew Rate,	1
3.5	Logical Effort: Predicting Delay, Logical Area and logical efficiency	1
3.6	Logical path, Multistage cells,	1
3.7	Optimum delay, Optimum number of stages, Library Cell Design	1
3.8	Library Architecture, Gate Array Design, Standard Cell Design, Data Path Cell design	1
4	**Programmability-8 hours**	
4.1	Programmable ASICs- Antifuse,	1
4.2	Static Ram, EPROM and EEPROM Technology	1

4.3	Practical issues, Specifications, Programmable ASIC logic cells: Actel ACT	1
4.4	Xilinx LCA, Altera Flex, Altera Max,	1
4.5	Programmable ASIC I/O cells: DC output,	1
4.6	AC Output, DC Input, AC Input, Clock Input	1
4.7	Power Input	1
4.8	Xilinx I/O block	1
5	**Devices and Synthesis-8 hours**	
5.1	Programmable ASIC Interconnect	1
5.2	Actel ACT, Xilnx LCA	1
5.3	Xilinx EPLD	1
5.4	Altera Max 5000 and 7000	1
5.5	Altera Max 9000	1
5.6	Altera Flex, VHDL	1
5.7	Verilog HDL	1
5.8	Logic Synthesis.	1

CODE	COURSE	CATEGORY	L	T	P	CREDIT
24SJ1EE C043	EMBEDDED OPERATING SYSTEM	PROGRAM ELECTIVE II	3	0	0	3

Preamble: The purpose of this course is to provide a complete awareness of Embedded Operating Systems and Embedded Software Development. As an outcome of the course the students will be ready for OS porting, Embedded baremtal application development, Linux device driver development and RTOS porting

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Student will be enabled to write, compile and run baremtal application programs for embedded systems. **(Cognitive Knowledge Level: Apply)**
CO 2	Student will get knowledge on Operating systems internals like scheduling, memory management etc. **(Cognitive Knowledge Level: Analyse)**
CO 3	Introduction to an RTOS named FreeRTOS and familarization on developement of real world application on FreeRTOS **(Cognitive Knowledge Level: Apply)**
CO 4	Student will acquire knowledge on Linux internals, kernel modules, libraries, root file system etc. **(Cognitive Knowledge Level: Analyse)**
CO 5	Student will be able to develop and run basic Linux device drivers **(Cognitive Knowledge Level: Apply)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards

PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2			1				2	
CO 2	2	1	2		2	2	2	2	2
CO 3	2			2	2			1	2
CO 4		1	2				2	1	2
CO 5	2		2		2				1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination (%)
Apply	40	40
Analyse	35	35
Evaluate	25	25
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ**1EEC043 Course**

Name: Embedded Operating Systems

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Define the terms host and target machines, native and cross compilers?
2. Explain shared data, atomic and critical sections
3. What is the difference between hard real time and soft real time systems?
4. Explain the terms Kernel root file system, libraries, kernel modules and device files
5. Explain different types of Linux device drivers

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Develop and compile a program in assembly and C language for ARM/ RISC-V architecture
7. Develop and compile a program in C language for ARM/ RISC-V architecture and debug the program on Instruction Set Simulator
8. Explain advantages and disadvantages of different Software Architectures like Round Robin, Function Que scheduling etc.

9. Explain a scenario on critical sections and provide its solution
10. Write a C program for FreeRTOS demonstrating a real world application for RTOS
11. Create a rootfs structure for Linux and build the same for ARM /RISC-V
12. Write character and block device drivers, build for ARM/ RISC-V and test on an Instruction set simulator like QEMU

(5x7=35 Marks)

Syllabus

Module 1 (Embedded Software Development)

Host and Target Machines, Toolchain for Embedded Software, Native versus cross compilers, Using a standard library, C extensions for Embedded Systems, Getting Embedded Software into the target system, Debugging Techniques, Testing on your host machine, Instruction Set Simulators, Baremetal programming, IDEs

Module 2 (Operating Systems)

What are Operating Systems, Operating System Internals, Multitasking Operating Systems, Scheduling, Scheduler Algorithms, Memory Management, Interrupts and its significance in real time processing, saving and restoring context, disabling interrupts, characteristics of shared data, atomic and critical sections, interrupt latency. Software Architectures: Round Robin, Round Robin with interrupts, Function Queue scheduling Architecture, Architecture selection.

Module 3 (Real Time Operating Systems)

Introduction to RTOS, Task and task states, Task and data, Semaphore and shared data. RTOS Architecture, Hard real time and Soft real time, Examples of Commercial RTOS RTOS Services: Message Queues, Mail boxes and pipes, Timer functions, events, Memory Management. Basic Design using an RTOS: Principle, Hard real time scheduling considerations, saving memory space, saving power, Real time application development using FreeRTOS.

Module 4 (Linux)

Linux Kernel, Linux internals, Kernel Considerations- selection, configuration , Compiling and Installing the Kernel Root File System structure, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization,Porting Kernel. Busy box, Root Filesystem Setup: Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk , Rootfs and Initramfs, Choosing a Filesystem's Type and Layout

Module 5 (Linux Device Drivers and Bootloaders)

Introduction, Building and running modules, Character Drivers, Block device drivers, Net device drivers, Allocating memory. USB Drivers, Device Model, Memory mapping and

DMA, Block Drivers, TTY Drivers. Setting Up the Bootloader: Embedded Bootloaders, Server Setup for Network Boot, Using the U-Boot Bootloader.

Reference Books

1. Steve Heath, Embedded System Design, 2nd edition, Newnes.
2. David Simon Embedded Software Primer, Addison- Wesley, 1999.
3. Dr.K V K K Prasad, Embedded / Real time systems: Concepts, Design and Programming, Dream Tech press, New Delhi.
4. Frank Vahid,Tony D. Givargis, Embedded System Design- A Unified Hardware/ Software Introduction, John Wiley and Sons, Inc 2002.
5. D Jonathan W. Valvano,Embedded Microcomputer systems, Brooks / Cole, Thompson Learning. New Jersey.
6. Arnold S Burger, Embedded Systems Design - Introduction to Processes, Tools, Techniques", CMP books
7. Daniele Lacamera, Embedded Systems Architecture, O'Reilly
8. Max Back, freeRTOS: A practical approach with Arduino
9. Daniel P. Bovet & Marco Cesati, Understanding the Linux Kernel, O'Reilly
10. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman, Linux Device Drivers

Course Plan

No	Topic	No. of Lectures
1	**Embedded Software Development**	**8 hours**
1.1	Host and Target Machines, Toolchain for Embedded Software	1
1.2	Native versus cross compilers, Using a standard library	1
1.3	C extensions for Embedded Systems	1
1.4	Getting Embedded Software into the target system	1
1.5	Debugging Techniques	1
1.6	Testing on your host machine, Instruction Set Simulators	1
1.7	Baremetal programming	1
1.8	IDEs	1
2	**Operating Systems**	**8 hours**
2.1	What are Operating Systems, Operating System Internals	1
2.2	Multitasking Operating Systems, Scheduling	1
2.3	Scheduler Algorithms, Memory Management	1
2.4	Interrupts and its significance in real time processing	1
2.5	saving and restoring context, disabling interrupts,characteristics of shared data	1
2.6	atomic and critical sections, interrupt latency	1

2.7	Software Architectures: Round Robin, Round Robin with interrupts	1
2.8	Function Queue scheduling Architecture, Architecture selection	1
3	**Real Time Operating Systems**	**8 hours**
3.1	Introduction to RTOS, Task and task states	1
3.2	Task and data, Semaphore and shared data	1
3.3	RTOS Architecture, Hard real time and Soft real time, Examples of Commercial RTOS	1
3.4	RTOS Services: Message Queues, Mail boxes and pipes	1
3.5	Timer functions, events, Memory Management	1
3.6	Basic Design using an RTOS: Principle, Hard real time scheduling considerations, saving memory space, saving power,	1
3.7	Real time application development using FreeRTOS	1
3.8	Real time application development using FreeRTOS	1
4	**Linux**	**8 hours**
4.1	Linux Kernel, Linux internals	1
4.2	Kernel Considerations- selection, configuration	1
4.3	Compiling and Installing the Kernel Root File System structure	1
4.4	Libraries, Kernel Modules, Kernel Images, Device Files	1
4.5	Main System Applications, Custom Applications, System Initialization, Porting Kernel.	1
4.6	Busy box, Root Filesystem Setup: Filesystem Types for Embedded Devices	1
4.7	Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem	1
4.8	Placing a Disk Filesystem on a RAM Disk , Rootfs and Initramfs, Choosing a Filesystem's Type and Layout	1
5	**Linux Device Drivers and Bootloaders**	**8 hours**
5.1	Introduction, Building and running modules	1
5.2	Character Drivers	1
5.3	Block device drivers	1
5.4	Net device drivers, Allocating memory	1
5.5	USB Drivers, Device Model, Memory mapping and DMA	1
5.6	Block Drivers, TTY Drivers	1
5.7	Setting Up the Bootloader: Embedded Bootloaders, Server Setup for Network Boot	1
5.8	Using the U-Boot Bootloader	1

24SJ1EEC011	REAL TIME OPERATING SYSTEMS	CATEGORY	L	T	P	CREDIT
		PE II	3	0	0	3

Preamble: Nil

Course Outcome

CO 1	Summarize the functions and structure of general-purpose operating systems.
CO 2	Use different scheduling algorithms on processes and threads.
CO 3	Interpret a real time operating system along with its synchronization, communication and interrupt handling tools.
CO 4	Illustrate task constraints and analyze the different scheduling algorithms on tasks.
CO 5	Illustrate the applications of real time operating systems.

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2
CO1	2	1						2	
CO2	2		2	2	2	2	2	2	2
CO3	2	2			2			2	2
CO4			2	2		1	2	1	2
CO5	2		2		2				1

Assessment Pattern:

Bloom's Category	CIE	End Semester Examination
Apply	10	20
Analyse	10	20
Evaluate	20	20
Create		

Mark distribution:

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 Hours

Continuous Internal Evaluation Pattern:

The evaluation shall only be based on application, analysis, or design-based questions (for both internal and end-semester examinations)

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed original publications (minimum 10publications shall be referred): 15 marks
Course based task/Seminar/Data collection and interpretation: 15 marksTest paper, 1 no.: 10 marks
Test paper shall include minimum 80% of the syllabus.

End Semester Examination: 60 marks

The end semester examination will be conducted by the Institute . There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 5 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module ofwhich student shall answer any five. Each question can carry 7 marks. Total duration of the examination will be 150 minutes.

Syllabu

s

Module I (6)

Operating system: Types, Objectives and functions , Kernel, Process - States, Process Control Block, Operations on processes

Module II (7)

Process Scheduling: FCFS, SJF, Priority, Round-Robin, Multilevel Queue and Multilevel Feedback Queue Scheduling. Thread: Structure.User and kernel level threads, multi-threading models, multiprocessor scheduling

Module III (8)

Real Time Operating Systems: Structure and characteristics of Real Time Systems, Task: Task states, Task synchronization -Semaphores- types, Inter task communication mechanisms: message queues, pipes, event registers, signals, Exceptions and interrupt handling.

Module IV (8)

Task constraints, Task scheduling: Aperiodic task scheduling: EDD. EDF, LDF, EDF with precedence constraints. Periodic task scheduling:Rate monotonic and Deadline monotonic, Real time Kernel- Structure, State transition diagram, Kernel primitives

Module V

Features of Free RTOS and Linux.
Commercial real time operating systems: PSOS, VRTX, RT Linux-
Case study of (Kernel design, threads and task scheduling) RTOS: MicroC/OS-II. RTOS control system used in real life applications - in adaptive cruise control

Text Books

1. Abraham Silberschatz- 'Operating System Principles': Wiley India,7th edition, 2011
2. William Stallings –'Operating systems- Internals and design principles', Prentice Hall, 7th edition, 2011
3. Qing Li – 'Real-Time Concepts for Embedded Systems ', CMP Books, 2013 4.Giorgio C. Buttazzo, -'HARD REAL-TIME COMPUTING SYSTEMS PredictableScheduling Algorithms and Applications', Kluwer Academic Publishers.
5. Tanenbaum -'Modern Operating Systems' ,Pearson Edition, 3/e, 2007.
6. Jean J Labrosse , 'Micro C/OS-II, The Real Time Kernel' , CMP Books, 2011
7. Rajib Mall, 'Real-Time Systems: Theory and Practice ', 2008.
8. David E. Simon 'An Embedded Software Primer', Pearson 2012
9. Raj Kamal, 'Embedded Systems – Architecture, Programming and Design',Tata McGraw Hill

SEMESTER II

SLOT	COURSE CODE	COURSE NAME	MARKS		L-T-P	HOURS	CREDIT
			CIA	ESE			
A	24SJ2TEC100	FOUNDATIONS OF DATA SCIENCE	40	60	3-0-0	3	3
B	24SJ2TEC004	ANALOG VLSI DESIGN	40	60	3-0-0	3	3
C	24SJ2EECXXX	PROGRAM ELECTIVE 3	40	60	3-0-0	3	3
D	24SJ2EECXXX	PROGRAM ELECTIVE 4	40	60	3-0-0	3	3
E	24SJ2EECXXX	INDUSTRY/ INTERDISCIPLINARY ELECTIVE	40	60	3-0-0	3	3
S	24SJ2PEC100	MINI PROJECT	100	--	0-0-4	4	2
T	24SJ2LEC003	DESIGN LAB II	100	--	0-0-2	2	1
Total			**400**	**300**		**21**	**18**

Teaching Assistance: 6 hours

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2TEC100	FOUNDATIONS OF DATASCIENCE	DISCIPLINE CORE 2	3	0	0	3

Preamble: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand the basics of machine learning and different types.
CO 2	Differentiate regression and classification, Understand the basics of unsupervised learning and non-metric methods
CO 3	Apply statistical methods in non-linear classification and neural networks
CO 4	Understand the basics of deep learning networks, convolutional neural networks

Mapping of course outcomes with program outcomes (1-3)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2							2	
CO 2	2		2		2	2	2	2	2
CO 3	2				2			1	2
CO 4			2				2	1	2

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation : 40 marks
Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks
Test paper, 1 no. : 10 marks

End Semester Examination Pattern:
Total : 60 marks
Part A: Answer all – 5 questions x 5 marks : 25 marks
Part B: Answer 5 of 7: 5 questions x 7 marks : 35 marks

The end semester examination will be conducted by the Institute . There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question
(such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

Total: 60 marks

Part A (Answer all) **25 marks**

1. Discuss different types of machine learning with examples. (5)
2. Differentiate regression and classification with examples (5)
3. How SVM is used for multiclass problem? (5)
4. Explain clustering with examples. (5)
5. Discuss different activation functions used in deep neural networks (5)

Part B (Answer any 5) **35 marks**

6. Explain the terms features, training set, target vector, test set, and curse of dimensionality in machine learning. (7)
7. Show that the Bayesian classifier is optimal with respect to minimizing the classification error probability. (7)
8. Give a step by step description of the perceptron algorithm in classification. (7)
9. Obtain the cost function for optimization in SVM for separable classes. (7)
10. Describe convolutional neural networks with detailed description of each layers (7)
11. Obtain the decision surface for an equi-probable two class system, where the probability density functions of n-dimensional feature vectors in both classes are normally distributed. (7)
12. Explain the principle of back propagation neural networks with neat architecture diagram (7)

Syllabus and Course Plan (total hours: 37)

No	Topic	hours
1	**8 hours**	
1.1	Basics of machine learning, supervised and unsupervised learning,examples,	2
1.2	features, feature vector, training set, target vector, test set	1
1.3	over-fitting, curse of dimensionality.	1
1.4	Evaluation and model selection: ROC curves, evaluation measures,	2
1.5	validation set, bias-variance trade-off.	1
1.6	confusion matrix, recall, precision, accuracy.	1
2	**7 hours**	
2.1	Regression: linear regression, error functions in regression	1
2.2	multivariate regression, regression applications, bias and variance.	1
2.3	Classification : Bayes' decision theory,	2
2.4	discriminant functions and decision surfaces,	1
2.5	Bayesian classification for normal distributions, classification applications.	2
3	**7 hours**	
3.1	Linear discriminant based algorithm: perceptron, perceptron algorithm,	1
3.2	support vector machines.	2
3.3	Nonlinear classifiers, the XOR problem,	2
3.4	multilayer perceptrons,	1
3.5	backpropagation algorithm.	1
4	**8 hours**	
4.1	Unsupervised learning:	1
4.2	Clustering, examples, criterion functions for clustering,	2
4.3	proximity measures, algorithms for clustering.	1
4.4	Ensemble methods: boosting, bagging.	2
4.5	Basics of decision trees, random forest, examples.	2
5	**7 hours**	
5.1	Introduction to deep learning networks,	1
5.2	deep feedforward networks,	2
5.3	basics of convolutional neural networks (CNN)	2
5.4	CNN basic structure, Hyper-parameter tuning, Regularization - Dropouts,	1
5.5	Initialization, CNN examples	1

Reference Books

1. Bishop, C. M. "Pattern Recognition and Machine Learning" Springer, New York, 2006.
2. Theodoridis, S. and Koutroumbas, K. "Pattern Recognition". Academic Press, San Diego, 2003.
3. Hastie, T., Tibshirani, R. and Friedman, J. "The Elements of Statistical Learning". Springer.

4. Duda, R.O., Hart, P.E., and Stork, D.G. “Pattern Classification”. Wiley, NewYork,

5. Ian Goodfellow, Yoshua Bengio, Aaron Courville. “Deep Learning” MIT Press, 2016

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2TEC 004	ANALOG VLSI DESIGN	PROGRAMCORE 3	3	0	0	3

Preamble: The Analog VLSI Design course focuses on developing the knowledge and analytical skills required for designing and analyzing CMOS analog circuits. The student will gain an in depth knowledge in the operation of MOS transistors, acquire the knowledge of the analysis and design of CMOS circuit including basic building blocks of CMOS circuits, amplifiers etc. The student will gain a glance into the operation and design of advanced circuits.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	To the understand operation of MOSFET, IV Characteristics, small signal and large signal models and perform analysis
CO 2	Ability to analyze and design basic analog components including single stage amplifiers and current mirrors
CO 3	Ability to analyze and understand frequency response and noise sources in circuits
CO 4	Ability to design and analyze various single and multi stage operational amplifiers
CO 5	Gain understanding on the architecture and working of complex circuits such as PLL, comparators etc

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	2							2	
CO 2	2		2		2	2	2	2	2
CO 3	2				2			1	2
CO 4			2				2	1	2
CO 5		2	2	1	1			1	

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40
Analyse	20
Evaluate	20
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 20 marks

Course based task/Seminar/Quiz : 10 marks Test

paper, 1 no. : 10 marks

The project shall be done individually. Group projects not permitted. Test papershall include minimum 80% of the syllabus

End Semester Examination Pattern:

The end semester examination will be conducted by the Institute . There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students),with 1 question from each module, having 5 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem-solving, and quantitative evaluation), with minimum one question from each module of which student shall answer any five. Each question can carry 7 marks. The total duration of the examination will be150 minutes

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

Marks: 60 marks **Duration: 2.5 hours**

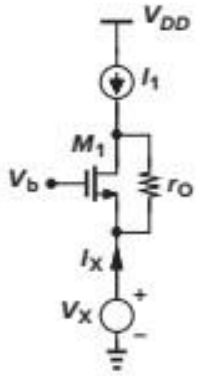
PART A

Answer all Questions: 5 marks each – 5 x 5 = 25 marks

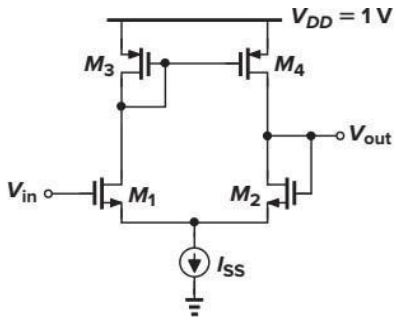
1. With the help of a diagram explain the small signal model of a NMOS transistor considering the effect of channel length modulation and body effect

2. Analyze and compare the gain and output impedance of a common source amplifier with resistive load and an ideal current source load with the help ofsmall signal models of the amplifiers.

3. Using millers theorem compute the input impedance of common gate amplifier shown in the figure below



4. Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer shown in the image below



5. With the help of diagrams explain the working of an XOR phase detector (PD). If the output swing is Vo, plot the input output characteristics of thePD. Calculate the gain of the XOR based PD from the output characteristics.

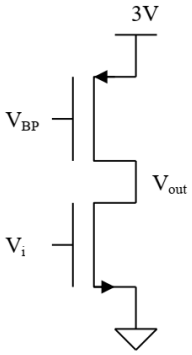
PART B

Answer any 5 Questions: 7 marks each - 5 x 7 = 35 marks

6. a) Consider a NMOS transistor with the parameters W/L = 100u/1u, with $\mu_n C_{ox}$ = 100uA/V², VDD = 3V, λ = 1/(10V), and V_{TH} = 1V. Carefully sketch by hand the drain current I_D vs. VDS. VDS has to swept from 0 to 3V at constant VGS=0, 1, 2, 3V. (calculations must be shown)

   b) Consider a PMOS transistor with the parameters W/L = 100u/1u, with $\mu_p C_{ox}$ = 100uA/V², VDD = 3V, λ = 1/(10V), and V_{TH} = -1V. Carefully sketch by hand the drain current I_D vs. VDS. VDS has to swept from 0 to -3V at constant VGS = 0, -1, -2, -3 V. (calculations must be shown)

7. For a common source amplifier shown in figure below assume the following parameters: $\mu C_{ox}(W/L)$ =1mA/V² , |Vt|=1V, and λ = 0.1V⁻¹ for both devices

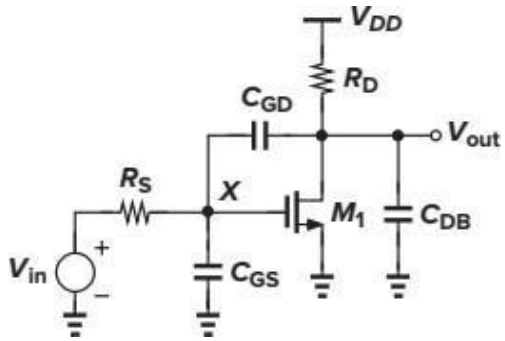


a) Assuming V_{BP} = 1.8 V, calculate V_{dsatp} and I_{dp} at V_{dp}=VDD-|V_{dsatp}| for the PMOS transistor.

b) Plot |I_{dp}| vs. Vout. What is the minimum and maximum value for Idp withthe PMOS device in saturation in this circuit?

c) What is the value of Vi for which the NMOS device leaves saturation?

8. For a common source amplifier shown in figure estimate the input pole, output pole and transfer function of the circuit(use miller theorm)



9. Design a 2-stage NMOS input CMOS op-amp with the following specs:

   - 200uA tail current
   - able to sink 1mA from the load

- output swing to within 200mV of the rails
- input common mode range to within 200mV of the top rail, and 1.4V of the bottom rail.

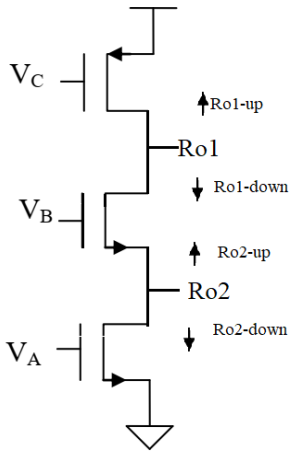
Process specs $\mu_n C_{ox}$ = 200uA/V^2, $\mu_p C_{ox}$=100uA/V2, λ =1/(10V), Vthp = -1V, Vthn = 1V, VDD = 5V, Lmin = 0.5um, Oxide capacitance Cox=5fF/um^2, Overlap capacitance Cov = 0.5fF/um. No ideal current sources are to be used in the design. The bias for the first stage tail must be generated using acurrent mirror with a resistive load.

Draw the schematic, label the device size of each transistor and the bias current flowing in each leg.

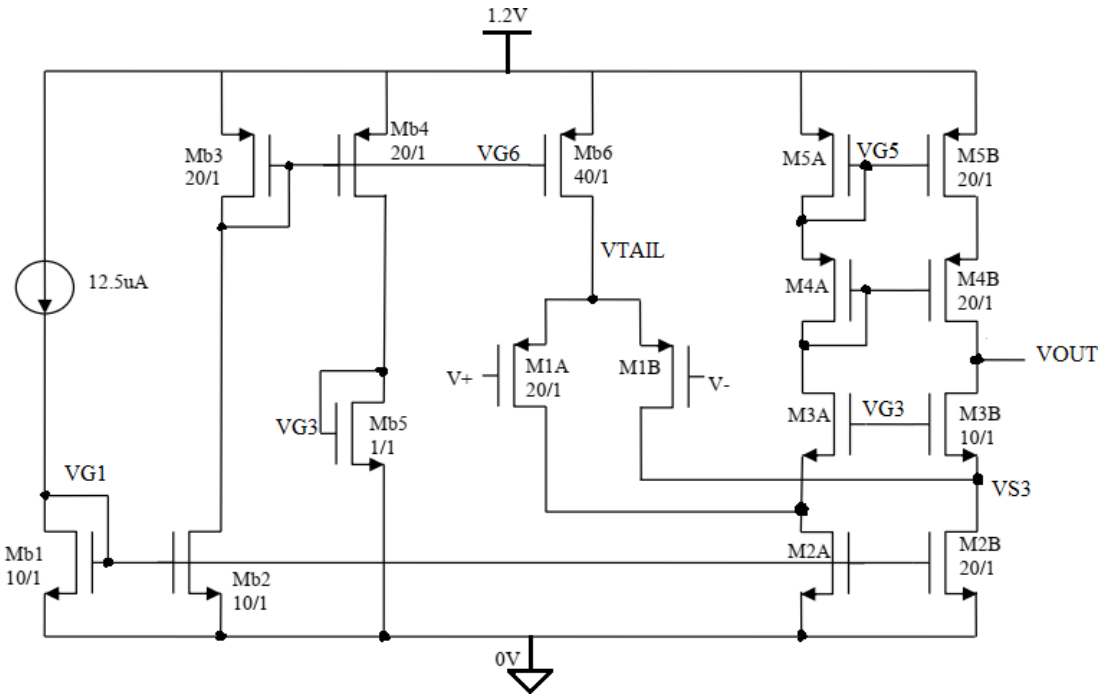
Calculate the 1st and 2nd stage gain, and the overall differential mode gain

10. Explain the concept for the generation of the negative and positive temperature coefficient sources with simple circuit diagram. Explain with the help of a circuit diagram how the positive and negative temperature confident sources can be combined to create and temperature independent voltage reference.

11. What is the low frequency impedance seen "looking up" and "looking down" at the output nodes Ro1 and Ro2 indicated in the circuit? Assume that all nmos devices have transconductance g_{mn} and output resistance r_{on}, and all pmos devices have transconductance g_{mp} and output resistance r_{op}. Write your answer in terms of g_{mp} , g_{mn}, r_{on}, and r_{op}. Write the full expression for up and down resistances Ro1-up, Ro1-down, Ro2-up and Ro2-down. Use small signal models to derive the same.



12. For the PMOS-input folded cascode op-amp below, assume quadratic model and the following process specs $\mu_n C_{ox}$ = 250uA/V^2, $\mu_p C_{ox}$ = 125uA/V^2, λ = 1/(10V), Vtp = -0.2V, Vtn = 0.2V, Oxide Capacitance Cox = 5fF/um^2, Overlap capacitance Cov = 0.5fF/um



a) Calculate the following operating point bias conditions
   i) The overdrive voltage and current in all devices. For this step assume that $\lambda = 0$
   ii) Calculate the bias voltages on all nodes VG1, VG3, VG6, VTAIL, VG5, VS3 and VOUT
   iii) The gm and ro parameters for M1 through M5
b) Calculate Gm, Ro, Av, input common mode range and output swing

Syllabus and Course Plan

(For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for30 hours).

No	Topic	No. of Lectures
1	**MOS Device Basics and Operation:**	
1.1	• MOS I/V Characteristics: Threshold voltage, derivationof I/V characteristics, regions of operation, MOS Transconductance.	1
1.2	• Second order effects: Body effect, Channel Length Modulation, Sub Threshold Conduction	1
1.3	• MOS Device Models: MOS device capacitances, MOS large signal model, MOS small signal model-basic, with channel length modulation, with body effect	2

1.4	• MOS Scaling Theory • MOS Short Channel Effects: Threshold Voltage Variation, Mobility degradation, velocity saturation, Hot carrier effects, Output impedance variation	1
2	**Basic MOS circuits:**	
2.1	• Single Stage Amplifiers: Common Source(CS) amplifier – Large signal and small signal behaviour with resistive load, diode connected load and current source load; CS amplifier with source degeneration • Source follower • Common gate stage	3
2.2	• Differential Amplifiers: Basic Differential Pair-large signal and small signal behaviour, Common Mode response • Differential Pair with MOS Loads	2
2.3	• Current Mirrors: Analysis and characteristics of Basic Current Mirror and Cascode Current Mirror • Active Current Mirrors: Differential pair(5 transistor OTA) with active load- large and small signal analysis	3
3	**Frequency response of circuits**	
3.1	• Frequency Response- Miller effect, bode plot, poles and zeroes, gain and phase margins , association of poles with nodes	2
3.2	• Analysis of common source amplifier frequency response • Analysis of common gate amplifier frequency response	3
3.3	• Analysis of frequency response of differential pair with active load	2
4	**Operational Amplifiers:**	
4.1	• Opamp Performance parameters • One stage op-amp topologies: characteristics and design of basic one stage opamp, telescopic cascode and folded cascode opamp	3
4.2	• Two stage Opamps: analysis and design of basic two stage topology and two stage telescopic cascode topology	2
4.3	• Common mode feedback (CMFB): basic concept • Common mode sensing in single stage opamp: (resistive feedback, source follower) • CMFB feedback techniques in single stage opamp	2
4.4	• Frequency compensation: need for compensation, Barkhausen's Criteria , root locus • Basic principle of compensation in a single stage telescopic cascode opamp • Miller compensation in two stage amplifier	3
5	**Advanced CMOS circuits:**	

5.1	• Temperature independent reference: Concepts and basic topology of positive temperature coefficient, negative temperature coefficient and bandgap reference	1
5.2	• Basic CMOS comparator: basic comparator circuit topology with pre-amplification, decision and output buffer stages [Reference book 3]	2
5.3	• Phase Locked Loops-Simple PLL(topology and dynamics), Charge pump PLL(topology and dynamics),	3
5.4	• MOS Sampling switches, resistance equivalence of parallel switched capacitor • Switched Capacitor unity gain buffer- basic topology and working • Non inverting Switched capacitor integrator - basic topology and working [Reference book 2]	4

Reference Books

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata McGraw HILL, 2nd Edition 2015.
2. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford Institute Press, 2002.
3. R. Jacob Baker, CMOS circuit Design Layout and Simulation, 3rd Edition.
4. David. A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
5. Paul B Gray and Robert G Meyer, Analysis and Design of Analog Integrated Circuits 4th Edition.

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2PEC 100	MINI PROJECT	PROJECT	0	0	4	2

Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The ultimate aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem solving skills.

The introduction of mini projects ensures preparedness of students to undertake dissertation. Students should identify a topic of interest in consultation with PG Programme Coordinator that should lead to their dissertation/research project. Demonstrate the novelty of the project through the results and outputs.The progress of the mini project is evaluated based on three reviews, two interim reviews and a final review. A report is required at the end of the semester.

Evaluation Committee - Programme Coordinator, One Senior Professor and Guide.

Sl. No	Type of evaluations	Mark	Evaluation criteria
1	Interim evaluation 1	20	
2	Interim evaluation 2	20	
3	Final evaluation by a Committee	35	Will be evaluating the level of completion and demonstration of functionality/specifications, clarity of presentation, oral examination, work knowledge and involvement
4	Report	15	the committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level(not more than 25%)
5	Supervisor/Guide	10	
	Total Marks	100	

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2LEC003	DESIGN LAB II	LABORATORY 2	0	0	2	1

Preamble: The purpose of this course is to provide a solid foundation that furnishes the learner with in-depth knowledge of VLSI, Embedded systems and Signal processing. The students will be able to study and practice various tools for the VLSI design, FPGA programming, Embedded system design and signal processing. They can find solutions to real-world problems by completing this course in which they will be exposed to various hardware platforms and software tools for design, synthesis and simulation.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Study various VLSI design tools and find solution for a given problem **(Cognitive Knowledge Level: Evaluate)**
CO 2	Study various Embedded system design tools and find solution for a given problem. **(Cognitive Knowledge Level: Evaluate)**
CO 3	Study various Signal Processing tools and find solution for a given problem. **(Cognitive Knowledge Level: Evaluate)**
CO 4	Identify a practical problem and develop a solution. Test, simulate andrealise the solution **(Cognitive Knowledge Level: Create)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards

PO 5	An ability to identify, select and apply appropriate techniques, resourcesand state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and developmentrelated to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1			2	2	2			1	1
CO 2			2	2	2			2	2
CO 3			2	2	2			2	2
CO 4	2	1				1	3	2	1

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation
Apply	20
Analyze	20
Evaluate	20
Create	40

Mark distribution

Total Marks	Continuous Internal Evaluation	End Semester Examination
100	100	--

Continuous Internal Evaluation Pattern (Laboratory):

The laboratory courses will have only Continuous Internal Evaluation and carry 100 marks. The final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

List of Experiments

The following experiments are to be completed by designing a solution for the problem in software or hardware. The solution may be tested and debugged so that it can be implemented in real time. Minimum of fifteen experiments are to be completed from the list given below.

	Part A	
	The following experiments are to be completed by using any VLSI tool.	
Sl No	**Experiment Title**	**CO Mapping**
1	Rising edge detector (moore/mealy based design)	CO1
2	Debouncing circuit based on RT methodology	CO1
3	Dual edge detector (moore/mealy based)	CO1
4	Design, coding, functional simulation and synthesis of a priority encoder that returns the codes of the highest and second-highest priority requests.	CO1
5	FPGA implementation of a pre-loadable gray counter	CO1
6	Realization of a Real Time Clock in the FPGA developmentboard	CO1
7	Design, HDL coding and implementation of a running displayon seven segment display.	CO1
8	Write HDL codes to design FIR/IIR filters in direct and transpose forms and demonstrate it using software simulationor hardware implementation.	CO1
9	Realise any of the following experiment using software simulation or hardware implementation 1. Voting machine 2. Traffic light controller. 3. Vending machine 4. ECG/EEG denoising filter	CO1
10	CMOS: Transient analysis	CO1
11	CMOS: Layout and verification of DRC	CO1
12	CMOS: LVS checking and Extract RC	CO1
13	CMOS : Delay calculation	CO1

14	Physical Design of digital logic circuits: Verilog simulation & Synthesize	CO1
15	Physical Design of digital logic circuits: Floor Planning, Power Planning & Placement	CO1
16	Physical Design of digital logic circuits: CTS and Timing	CO1
17	Physical Design of digital logic circuits: Routing, Verification & GDS export	CO1
18	System Verilog Experiments 1. Verification of FIFO 2. Verification of priority encoder	CO1
19	Analog Experiments 1. Current Mirror 2. Common Source Amplifier	CO1
20	Analysis of Differential amplifier	CO1
	Part B	
	The following experiments are to be completed using any Microcontroller by software or hardware tool.	
1	Develop a program to blink an LED with a 1 second delayusing a Real-Time Clock (RTC)	CO2
2	Develop a program to generate a square wave with a frequencyof 500Hz and 50%	CO2
3	Develop a program to interface two 7 segment displays and implement a stopwatch.	CO2
4	Develop a program to generate a sine wave of frequency 50Hz, sample it using ADC and reconstruct the sine wave using DAC	CO2
5	Develop a program to generate a square wave using PWMmodule and control its duty cycle	CO2
6	Develop a program to generate 50Hz sine wave on GPIO;connect to ADC input, filter using FIR, output using DAC	CO2
7	Develop programs for below given UART implementations 1. Transmit “Hello World” 2. Loopback test	CO2
8	Develop a program to implement a random number generator	CO2
9	Develop a program to implement I2C communication	CO2
10	Develop a program to implement SPI communication	CO2

11	Develop a program to control LED brightness using a variable resistor	CO2
12	Develop a program to interface a temperature sensor and display the temperature in an LCD.	CO2
13	Interface an EEPROM and develop a menu driven programthrough UART 1. Menu a. Read b. Write c. Erase	CO2
14	Interface a DC motor and develop a program to control 1. Forward motion 2. Reverse motion 3. Speed control	CO2
15	Interface a Stepper motor and develop a program to control 4. Forward motion 5. Reverse motion 6. Speed control	CO2
16	Interface and develop a program to 1. Display on an LCD/OLED 2. Read/ write to an SD Card	CO2
17	Interface and develop program 1. Configuring an external RTC (DS3231) 2. Communicate using CAN/RS485	CO2
18	Design and develop any one from the following 1. Voting machine 2. Traffic light controller 3. Vending machine 4. Home automation	CO2
19	Develop a C application to toggle the LED connected to GPIO on an OS ported development board.	CO2
20	Develop a device driver to toggle the LED connected to GPIO on an OS ported development board.	CO2
	Part C	
	The following experiments are to be completed using any signal processing tool.	
1	Linear Convolution, Circular Convolution and LinearConvolution using Circular Convolution.	CO3
2	To find the DFT and IDFT for the given input sequence.	CO3

3	FIR Filter (Low-pass, High-pass and Band-pass)design (Window method).	CO3
4	IIR Filter (Low-pass, High-pass and Band-pass)design (Butterworth and Chebychev).	CO3
5	Implementation of simple algorithms in Image enhancement – Negative, contrast stretching, power-law transformations etc	CO3
6	Implementation of simple Image filtering methods – Median , averaging, sharpening etc	CO3
7	Implementation of simple Image thresholding methods – hard thresholding, Otsu's algorithm	CO3
8	Implementation of Histogram processing – Equalization	CO3
9	Implementation of simple Image segmentation methods – K-means clustering, Region growing etc	CO3
10	Implementation of Hough transform	CO3
11	Study of sampling rate conversion (Decimation, Interpolation, Rational factor).	CO3
12	Wavelet decomposition of an Image – using Haar and Daubechies wavelets	CO3
13	Image denoising using wavelet transform	CO3
14	Image fusion – spatial and spectral methods	CO3
15	Image compression – JPEG, JPEG 2000, EBCOT etc	CO3
16	Familarization of DSP Hardware	CO3
17	Implementation of Linear convolution using DSP hardware	CO3
18	Implementation of FFT and IFFT of signals using DSP hardware	CO3
19	Implementation of FIR low pass filter using DSP hardware	CO3
20	Implementation of Overlap Save / Overlap Add Block Convolution using DSP hardware	CO3

Reference

1. Vinay K. Ingle, John G. Proakis, “Digital Signal Processing Using MATLAB.”
2. Allen B. Downey, “Think DSP: Digital Signal Processing using Python.”
3. Rulph Chassaing, “DSP Applications Using C and the TMS320C6x DSK
4. VEGA Processor

a. Datasheet : THEJAS32 SoC Datasheet

b. Development board : https://vegaprocessors.in/devboards/ariesv2.html

c. SDK user guide : https://cdac-vega.gitlab.io/sdkuserguide.html

5. TMS320F28335 datasheet.
6. LPC1769 datasheet.

SEMESTER II

PROGRAM ELECTIVE 3						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
C	1	24SJ2EEC035	EMBEDDED NETWORKING	3-0-0	3	3
	2	24SJ2EEC043	SoC DESIGN	3-0-0	3	3
	3	24SJ2EEC036	VLSI STRUCTURE FOR DSP	3-0-0	3	3
	4	24SJ2EEC037	SEMICONDUCTOR MEMORIES	3-0-0	3	3
	5	24SJ2EEC038	EMBEDDED SYSTEM DESIGN	3-0-0	3	3
	6	24SJ2EEC039	MULTIRATE SIGNAL PROCESSING AND WAVELETS	3-0-0	3	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC035	EMBEDDED NETWORKING	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: The purpose of this course is to provide a solid foundation that furnishes the learner with in-depth knowledge of embedded networks. Students will get an overall idea regarding the protocols used in embedded systems and real time embedded systems. The syllabus covers basic protocols like UART and very advanced real time protocols like CAN. This course helps the learner to design an embedded system with various interfaces to I/O devices and peripherals as per the requirement and implement with a professional grade.

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO 1	Study the basic embedded protocols like UART and practical networks like RS232 and RS485. **(Cognitive Knowledge Level: apply, Analyse andcreate)**
CO 2	Study and design the basic embedded networks with popular protocols likeSPI and I2C **(Cognitive Knowledge Level: apply, Analyse and create)**
CO 3	Study a real time industrial grade embedded network CAN and try design areal time implementation with it. **(Cognitive Knowledge Level: apply and Analyse)**
CO 4	The most widely used network is based on LAN technologies. Student willbe able to study and create networks in LAN. **(Cognitive Knowledge Level: Apply and analyse)**
CO 5	Mobile hand sets and laptops are widely connected by wireless technologies. Students will be able understand and create networks based on wireless technologies. **(Cognitive Knowledge Level: apply, Analyse and create)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program

PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and developmentrelated to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation	End Semester Examination
Apply	40	40
Analyse	20	35
Evaluate	22	25
Create	20	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE:

PAGES: 3

Reg No:

Name:

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 222EEC035

Course Name: Embedded Networking

Max. Marks: 60
Duration: 2.5 Hours

PART A

Answer all Questions. Each question carries 5 Marks

1. What is the use of parity in communication? How odd and even parities are calculated?
2. Draw the standard CAN frame and mark various fields. Calculate the size ofa CAN frame if the size of the data is 7 bytes and the identifier is 11bits.
3. What are the signal levels in the idle lines of I2C? Explain the S and P conditions of the I2C communication.
4. An organization with 4 departments has the following IP address space: 11.3.22.0/23. It is required to create subnets to accommodate 4 departments. The subnets have to support to a minimum of 220, 64, 50, and 23 hosts respectively. What are the 4 subnet network numbers?

5. Consider the following loops, identify the true dependencies, outputdependences and anti-dependences and eliminate the output dependences and anti-dependences.

6. What is piggybacking in communication? Explain with an example.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

7. Calculate the bandwidth usage for CAN network with SYNC cycle time 33ms, Data length per message is 22 bytes and bus speed is 125kbps.
8. How synchronization is achieved in CAN communication? The following datais to be sent over the CAN bus. Show the timing diagram after the bit stuffing. 11000001111000011110.
9. In I2C bus what are the importance of ACK and NACK conditions? What are the conditions which generate a NACK status?
10. Draw frame format for IEEE802.3 LAN packet format. Calculate maximum and minimum size of a frame.
11. What is frequency hopping and paging in Bluetooth?
12. An organization with 4 departments has the following IP address space: 11.3.22.0/23. It is required to create subnets to accommodate 4 departments. The subnets have to support to a minimum of 220, 64, 50, and 23 hosts respectively. What are the 4 subnet network numbers?

(5x7=35 Marks)

Syllabus

Module 1 (Introduction)

Embedded Networking Requirements: Introduction to Network for Embedded Systems, Serial/Parallel Communication, Synchronous/Asynchronous Serial Protocols,
Serial communication protocols -UART, RS232, RS485.

Module 2 (SPI and I2C)

Synchronous Serial Protocols - SPI and I2C.
SPI : Introduction, Features, Modes of Operation , External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats, Baud Rate Generation, Error Conditions, Low Power Mode Options)
I2C : I2C-bus features, Modes of Operation - Standard-mode, Fast-mode, Fast- mode plus, Ultra fast mode. Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Clock Stretching, Addressing, Call Addresses, Reset, Device ID, Applications of I2C bus protocol.

Module 3 (CAN controller)

Controller Area Network : CAN Overview, Introduction, CAN 2.0b Standard. Physical Layer, Message Frame Formats, Bus Arbitration, Message Reception and Filtering, Error Management, Selecting a CAN Controller, CAN Development Tools.

Module 4 (LAN)

Elements of a LAN- Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed. OSI reference model, TCP/IP reference model. IP addressing, Subnetting.

TCP/IP: Introduction to TCP/IP: History, Architecture -layering, Standards and Applications,
Protocol Overview, Routers & Topology, IP routing, TCP Architecture, UDPArchitecture, Security Concepts.

Module 5 (Wireless Networks)

Wireless networks: Wifi - 802.11 standards, Architecture and protocol stack,Physical layer, MAC sublayer, 802.11 frame structure.
Bluetooth - Architecture, protocol stack - radio layer, link layers, frame structure.
Frequency hopping, piconets and scatternets.
Networking Examples - Home Automation. Block diagram, schematic, remotecontrol using IoT.

Reference Books

1. ANDREW S. TANENBAUM, "COMPUTER NETWORKS", FIFTH EDITION, Pearson Education, Inc., publishing as Prentice Hall. 2011
2. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.
3. Lyla B Das, “Embedded Systems-An Integrated Approach”, Pearson, 2012.
4. Olaf P Feiffer, Andrew Ayre & Christian Keyold, “Embedded Networking with CAN and CAN Open”, Embedded System Academy, 2005.
5. Marco Di Natale, Haibo Zeng, Paolo Giusto & Arakadeb Ghosal, “Understanding and Using the Controller Area Network” , Springer, 2012.
6. John Catsoulis, "Designing Embedded Hardware", O'Reilly Media, Inc., 2002.
7. Dr. Sidnie Feit, “TCP/IP : Architectures, Protocols and Implementations with IPv6 and IP Security”, Tata McGraw Hill, Second Edition, 2008.
8. Martin W. Murhammer, Orcun Atakan, Stefan Bretz,Larry R. Pugh, Kazunari Suzuki, David H. Wood, “TCP/IP Tutorial and Technical Overview”, International Technical Support Organization-IBM, Sixth Edition, October1998.

Syllabus and Course Plan

No	Topic	No. of Lectures
1	**Introduction**	**8 hours**
1.1	Embedded systems and Networking	1
1.2	Embedded Networking Requirements	1
1.3	Introduction to Network for Embedded Systems	1
1.4	Serial/Parallel Communication	1
1.5	Synchronous/Asynchronous Serial Protocols,	1
1.6	UART	1
1.7	RS232	1
1.8	RS485	1
2	**SPI and I2C**	**8 hours**
2.1	SPI : Introduction, Features, Modes of Operation , External Signal Description, xx)	1
2.2	External Signal Description,	1
2.3	Functional Description(Covering Master Mode, Slave Mode, Transmission Formats, Baud Rate Generation, ErrorConditions, Low Power Mode Options)	1
2.4	I2C : I2C-bus features, Modes of Operation - Standard-mode, Fast-mode, Fast-mode plus, Ultra fast mode.	1
2.5	Signals and Logic levels, Start/Stop conditions, byte format	1
2.6	Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration,	1
2.7	Clock Stretching, Addressing, Call Addresses	1
2.8	Reset, Device ID, Applications of I2C bus protocol	1
3	**CAN controller**	**8 hours**
3.1	Controller Area Network: CAN Overview	1
3.2	Introduction	1
3.3	CAN 2.0b Standard. Physical Layer	1
3.4	Message Frame Formats	1
3.5	Bus Arbitration	1
3.6	Message Reception and Filtering	1
3.7	Error Management	1
3.8	Selecting a CAN Controller, CAN Development Tools	1
4	**LAN**	**8 hours**

4.1	Elements of a LAN- Inside Ethernet – Building a Network Hardware options – Cables, Connections and network speed	1
4.2	OSI reference model	1
4.3	TCP/IP reference model	1
4.4	IP addressing	1
4.5	TCP/IP: Introduction to TCP/IP: History, Architecture - layering, Standards and Applications	1
4.6	Protocol Overview	1
4.7	Routers & Topology, IP routing	1
4.8	TCP Architecture, UDP Architecture, Security Concepts.	1
5	**Wireless Networks**	**8 hours**
5.1	Wireless networks: Wifi - 802.11 standards, Architecture and protocol stack, Physical layer, MAC sublayer	1
5.2	802.11 frame structure	1
5.3	Bluetooth - Architecture, protocol stack - radio layer, link layers	1
5.4	Frame structure	1
5.5	Frequency hopping	1
5.6	Piconets and scatter nets	1
5.7	Networking Examples - Home Automation. Block diagram,	1
5.8	Schematic, remote control using IoT	1

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC043	SoC DESIGN	PROGRAMMEELECTIVE 3	3	0	0	3

Preamble: Systems-on-Chip (SoCs) are at the core of most embedded computing and consumer devices. As a result, SoCs represent the fastest-growing segment of the semiconductor industry.The purpose of this course is to provide a solid foundation on System-on-Chips (SoCs) where many functions of an electronic system are integrated into a single chip. This course helps the learner to understand different components and design abstractions that contribute towards building complex systems, and apply this understanding to improve state-of-the-artSystem-on-Chip (SoC) designs. At the end of this program, a student would be able to appreciate and apply advances made across domains to design better SoCs.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study components of System on chip and its architecture. **(Cognitive Knowledge Level: Analyse)**
CO 2	Study System on chip design process, system level design issues and the concept of design reuse. **(Cognitive Knowledge Level: Analyse)**
CO 3	Study hard macro design process, familiarize with RTL coding guidelinesand macro synthesis guidelines. Use the knowledge gained to design various systems. **(Cognitive Knowledge Level: Apply)**
CO 4	Study Verification technology options, methodologies, and get familiarized with the SoC verification flow. Use the knowledge gained to design Testbenches for verification. **(Cognitive Knowledge Level: Apply)**
CO 5	Study MPSoCs, Techniques for designing MPSoC and understand the overview of SoC design flow with detailed application study. **(Cognitive Knowledge Level: Analyse)**
CO 6	Design and verification of SoC **(Cognitive Knowledge Level: Create)**

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher thanthe requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards

PO 5	An ability to identify, select and apply appropriate techniques, resources and state of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and developmentrelated to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	35
Analyse	30
Evaluate	25
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No. : 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE:

PAGES: 2

Reg No: Name:

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Name: System on chip design

Max. Marks: 60 Duration: 2.5 Hours

PART A

Answer all Questions. Each question carries 5 Marks

1. Differentiate between VLIW and Superscalar processors.
2. Specify the need of using reusable IP core and differentiate between Hard IP andSoft IP.
3. Explain briefly the design issues for hard macro.
4. Briefly explain block level verification and stress on its need.
5. What are the techniques used for controlling the power consumption of MPSoC.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Compare SOC interconnect methods.
7 Give a brief account of the logic design issues faced when designing for timingclosure.
8. Design a 4 bit up-down counter using VHDL and verify the functionality using a Testbench

9. Briefly explain the characteristics of a good IP.What are the main challenges faced while Integrating macros into the SoC design and explain the strategies for dealing with them?

10. You are required to develop a Set-Top Box SoC which inputs a signal andtransforms the data to content displayed on a TV screen. The target feature size is at the 65nm technology node. The Set-Top Box SoC architecture must consist ofthe following components: 64b CISC processor with 48KB of I-cache and 32KB of D-cache, A Texas Instrument DSP (for video signal acquisition), A SHARC-based DSP (for demodulation/ error correction schemes), MPEG-2 transport stream de- multiplexer accelerator unit, Bus and bus control, Application Memory (512KB), Shared SRAM L2 cache.Design an SoC based on the given specifications and also mention the SoC design flow.

11. Differentiate between Formal Model checking and Equivalence checking.

12. In the definition phase of a SoC architecture, a number of technical factors are considered for the implementation and mapping of the appropriate algorithms. Describe in detail with an application such as a 3 - D graphics engine, the factors you would consider essential for achieving your goal.

(5x7=35 Marks)

Syllabus and Course Plan

(For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for30 hours).

No	Topic	No. of Lectures
1	**Introduction to the Systems Approach**	8 Hours
1.1	System Architecture, Components of the System, Hardware and Software	2
1.2	Processor Architectures, Memory and Addressing, System-Level Interconnection	3
1.3	System Architecture and Complexity, Product Economics and Implications for SOC, Dealing with Design Complexity	3
2	**Design for reuse, System On Chip Design Process**	8 Hours
2.1	A canonical SoC Design, SoC,Design flow - waterfall vs. spiral	1
2.2	Top-down vs. Bottom up, Specification requirement, Types of Specification	1
2.3	System Design process, System level design issues- Soft IP vs. Hard IP	2
2.4	Design for timing closure, Logic design issues, Physical design issues	2
2.5	Macro Design Process- Overview, Key features, Planning and specification	1
2.6	Macro design and verification, Soft Macro productization	1

3	**Developing hard macros**	8 Hours
3.1	Design issues for hard macros, Design process	2
3.2	System Integration with reusable macros	2
3.3	RTL Coding Guidelines: Basic Coding Practices, Coding for Portability	2
3.4	Coding for Synthesis. Macro Synthesis Guidelines	2
4	**SoC Verification**	8 Hours
4.1	Verification technology options, Verification methodology	2
4.2	Verification approaches, System level verification	2
4.3	Block level verification, Hardware/software co-verification - Co-verification Environment	2
4.4	Macro Verification Guidelines-Verification Plan, Verification Strategy	1
4.5	Testbench Design, Timing Verification	1
5	**MPSoCs**	8 Hours
5.1	What, Why, How MPSoCs, Techniques for designing energy-aware MPSoCs- Energy-Aware Processor Design	2
5.2	Energy-Aware Memory System Design, Energy-Aware On-Chip Communication System Design	2
5.3	MPSoC performance modeling and analysis.	2
5.4	SoC Design Approach and application study	2

Reference Books

1. Computer System Design: System-on-Chip; Michael J. Flynn, Wayne Luk , ISBN: 978-1-118-00991-8 August 2011
2. Reuse Methodology Manual for System-On-A-Chip Designs, Springer, 32nd Edition, 2007
3. System-on-a-Chip Verification - Methodology and Techniques; Prakash Rashinkar, Peter Paterson, Leena Singh; 2002, Kluwer Academic Publishers
4. A.A.Jerraya, W.Wolf, Multiprocessor Systems-on-chips, M K Publishers.
5. RochitRajsuman, "System-on-a-chip: Design and Test ", Artech House, 2000 ISBN
6. Dirk Jansen,The EDA HandBook, Kluwer Academic Publishers.
7. William K.Lam, Design Verification: Simulation and Formal Method based Approaches,Prentice Hall.
8. Modern System-on-Chip Design on Arm; DAVID J. GREAVES, ARM Education Media, 2021

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC036	VLSI STRUCTURE FORDSP	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: The purpose of this course is to introduce students to the fundamentals of VLSI signal processing and applications. The Course describes the design and optimization of VLSI architectures for basic DSP algorithms.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Study the fundamentals of Pipelining.
CO 2	Evaluate parallel architectures useful in DSP implementation
CO 3	Apply Pipelining and Parallel processing of IIR systems
CO 4	Analyse fast convolution methods
CO 5	Understand Scaling and round off noise in filters.

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reportson complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resourcesand state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and developmentrelated to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation	End Semester Examination
Apply	40	40
Analyse	35	35
Evaluate	25	25
Create		

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marksTest paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Syllabus

Module-1

Review of Pipelining and parallel processing for FIR filters, algorithmic strength reduction-introduction, parallel FIR filters, Discrete Cosine Transform and inverse DCT

Module-2

Implementation of DCT and inverse DCT based on algorithm-architecture transformations.

Parallel architectures for Rank Order filters - Odd Even Merge sort architecture- Rank Order filter architecture-Parallel Rank Order filters-Running Order MergeOrder Sorter-Low power Rank Order filter.

Module-3

Pipelined and parallel recursive filters, Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-aheadpipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

Module-4

Fast convolution: Introduction, Cook-Toom Algorithm, Modified Cook-ToomAlgorithm, Winograd Algorithm, Iterated Convolution, cyclic convolution.

Module-5

Scaling and round off noise - Round off noise in pipelined IIR filters – round offnoise in lattice filters, pipelining of lattice IIR digital filters – low power CMOS lattice IIR filters

Reference Books

1. Keshab K. Parhi, VLSI Digital signal processing Systems: Design and Implementation, John Wiley & Sons, 1999.
2. Uwe meyer- Baes, DSP with Field programmable gate arrays, Springer, 2001
3. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
4. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.
5. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.

Model Question Paper

QP CODE: **PAGES:2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ2EEC036 Course

Name: VLSI Structures for DSP

Max. Marks: 60 Duration: 2.5 Hours

PART A

Answer all Questions. Each question carries 5 Marks

1. How transpose of a matrix in 2x2 linear convolution algorithm can be usedto obtain the 2 parallel filter.
2. Obtain the structure of time mapped rank order filter with W=8.
3. Write short notes on low power CMOS lattice IIR filters.
4. Obtain the matrix form of traditional 2 parallel FIR filter and draw itsstructure.
5. Explain Clustered look-ahead pipelining.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. State three steps of Algorithm-Architecture transformation. Prove that this method effectively reduces the number of multiplications in the implementation of 8-point DCT.
7. Consider the first order IIR filter with transfer function

   $H(Z)=1 / (1- az^{-1})$. Derive the filter structure with 4 level pipelining and 3 level block Processing.
8. Consider the odd-even merge based rank order filter with window size W=5. Assume that the filter is to be pipelined and total capacitance for one C&S

unit to be Co. a) What is the power consumption of a 3 parallel filter. b)What is the power consumption with substrate sharing implementation.

9. Consider a 2x3 linear convolution s(p)=h(p)x(p). where $h(p)=h_0+h_1p$, $x(p)=x_0+x_1p+x_2p^2$. Use Cook Toom algorithm to construct an efficient implementation for the given linear convolution.

10. Explain how round off noise is calculated in lattice filters and IIR filters.

11. Construct a 3 x 3 convolution using a 4 x 4 cyclic convolution algorithm.

12. Derive Fast 2^m-point DCT structure by the decimation-in-frequency approach.

(5x7=35 Marks)

Syllabus and Course Plan

No	Topic	No. of Lectures
1	**Module 1-8 hours**	
1.1	Review of Pipelining and parallel processing for FIR filters	2
1.2	Algorithmic strength reduction-introduction	2
1.3	parallel FIR filters	1
1.4	Discrete Cosine Transform	2
1.5	Inverse DCT	1
2	**Module-II -8 hours**	
2.1	Implementation of DCT and inverse DCT based on algorithm-architecture transformations.	2
2.2	Parallel architectures for Rank Order filters	1
2.3	Odd Even Merge sort architecture	1
2.4	Rank Order filter architecture	1
2.5	Parallel Rank Order filters	1
2.6	Running Order Merge Order Sorter	1
2.7	Low power Rank Order filter	1
3	**Module-III -8 hours**	
3.1	Pipelined and parallel recursive filters	1
3.2	Look-Ahead pipelining in first-order IIR filters	1
3.3	Look-Ahead pipelining with power-of-2 decomposition	1
3.4	Clustered look-ahead pipelining	1
3.5	Parallel processing of IIR filters	2
3.6	Combined pipelining and parallel processing of IIR filters.	2
4	**Module-IV -8 hours**	
4.1	Fast convolution: Introduction	1
4.2	Cook-Toom Algorithm	2
4.3	Modified Cook-Toom Algorithm	1

4.4	Winograd Algorithm	2
4.5	Iterated Convolution	1
4.6	Cyclic convolution	1
5	**Module-V -8 hours**	
5.1	Scaling and round off noise	2
5.2	Round off noise in pipelined IIR filters	1
5.3	Round off noise in lattice filters	1
5.4	Pipelining of lattice IIR digital filters	2
5.5	Low power CMOS lattice IIR filters	2

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC037	SEMICONDUCTOR MEMORIES	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: This course aims to impart the advance knowledge of memory devicesand enable students to design, test and debug the memory devices.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyse the different types of RAM and ROM design.
CO 2	Analyse the different RAM and ROM architecture and interconnect.
CO 3	Analyse about design and characterization techniques.
CO 4	Analysis of different memory testing and design for testability.
CO 5	Identification of new developments in semiconductor memory design

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	10
Analyse	40
Evaluate	10
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marksTest paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Syllabus

Module– I

Random Access Memory Technologies: Static Random Access Memories (SRAMs):SRAM cell structure MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, silicon on insulator (SOI) technology, advanced SRAM architectures and technologies, application specific SRAMs. **Dynamic Random Access Memories (DRAMs)**: DRAM technology development, CMOS CRAMs, DRAMs cell theory and advanced cell structures- BiCMOS DRAMs- soft error failure in DRAMs, Advanced DRAM designs and architecture, application specific DRAMs.

Module – II

Non-volatile Memories: Masked Read only memories (ROMs): High density ROMs, programmable read-only memories (PROMs)- bipolar PROMs, CMOS PROMs, erasable (UV)- Programmable read-only memories (EPROMs)- Floating Gate EPROM cell- one, time programmable (OTP) Eproms, Electrically Erasable PROMs (EEPROMs), EEPROM technology and architecture, non-volatile SRAM-Flash memories (EPROMs or EEPROM), Advanced flash memory architecture.

Module – III

Memory fault modelling, testing and memory design for Testability and fault tolerance, RAM fault modelling, electrical testing, Pseudo random testing, megabit DRAM testing non-volatile memory modelling and testing, IDDQ fault modelling and testing, application specific memory testing.

Module – IV

Semiconductor memory reliability: General Reliability issues, RAM failure modesand mechanism, non volatile memory reliability, reliability modelling and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification.

Module – V

Advanced memory technologies and high-density memory packagingtechnologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog memories, magneto resistive random access memories (MRAMs), Experimental memory devices. Memory hybrids and MCMs (2D), Memorystacks and MCMs (3D), Memory MCM testing and reliability issues- memory cards- high density memory packaging future directions.

Reference Books

1. Ashok K.Sharma, Semiconductor Memories Technology, testing and reliability, Prentice hall of India Private Limited, New Delhi 1997.
2. Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley 2002.
3. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill

Model Question Paper

QP CODE: **PAGES:1**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ2EEC037 Course Name: Semiconductor Memories.

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Draw and explain the SRAM cell Structure.
2. Draw the mask ROM development stages and explain..
3. What is bridging fault? .Explain with Supporting Data.
4. Briefly describe the main charge loss mechanisms in EPROM.
5. Differentiate the key differences between FRAMS and EEPROMs.

(5x5=25 Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Explain different types of application specific SRAMs.
7. Explain Advanced FLASH memory architectures with automatic Erase Algorithm.
8. Which are the most commonly used RAM Memory fault models? Expalin.
9. Explain General Semiconductor memory reliability issues.
10. Draw the FRAM cell structure and explain its operation.
11. Explain SRAM reliability issues.
12. Explain the soft error failures in DRAMs.

(5x7=35 Marks)

Syllabus and Course Plan

Unit No	Topic	No. of Lectures
1	**Random Access Memory Technologies**	
	(SRAMs): SRAM cell structure MOS SRAM architecture	1
	MOS SRAM cell and peripheral circuit operation	1
	bipolar SRAM technologies, silicon on insulator (SOI) technology	1
	silicon on insulator (SOI) technology, advanced SRAM architectures and technologies	1
	application specific SRAMs	1
	(DRAMs): DRAM technology development, CMOS CRAMs	1
	DRAMs cell theory and advanced cell structures- BiCMOS DRAMs	1
	soft error failure in DRAMs, Advanced DRAM designs and architecture	1
	application specific DRAMs.	1
2	**Non volatile Memories**	
	Masked Read only memories (ROMs): High density ROMs,	1
	programmable read-only memories (PROMs)- bipolar PROMs, CMOS PROMs	2
	erasable (UV)- Programmable read-only memories (EPROMs)- Floating Gate EPROM cell- one, time programmable (OTP) Eproms,	2
	Electrically Erasable PROMs (EEPROMs), EEPROM technology and architecture, non-volatile SRAM	2
	Flash memories (EPROMs or EEPROM), Advanced flash memory architecture.	2

3	**Memory fault modelling, testing and memory design for Testability and fault tolerance**	
	RAM fault modelling	1
	Electrical testing	1
	Pseudo random testing	1
	megabit DRAM testing non volatile memory modelling and testing	2
	IDDQ fault modelling and testing,	1
	application specific memory testing.	1
4	**Semiconductor memory reliability:**	
	General Reliability issues	1
	RAM failure modes and mechanism	1
	non volatile memory reliability	1
	reliability modelling and failure rate prediction	2
	design for reliability, reliability test structures, reliability screening and qualification	2
5	**Advanced memory technologies and high-density memory packaging technologies:**	
	Ferroelectric Random Access Memories (FRAMs)	1
	Gallium Arsenide (GaAs) FRAMs	1
	Analog memories ,magneto resistive random access memories (MRAMs)	2
	Experimental memory devices	1
	Memory hybrids and MCMs (2D), Memory stacks and MCMs (3D)	1
	Memory MCM testing and reliability issues	1
	memory cards- high density memory packaging future directions.	1

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC038	EMBEDDED SYSTEM DESIGN	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: The course, Embedded System Design, provides a substantial knowledge base in enabling the student to design complex embedded systems from scratch. Major topics covered in-depth are knowledge of various embedded system technologies with a stress on processor technologies, peripherals, and communication interfaces. The course also covers the aspects of hardware-software co-design and techniques for program modelling. The student will get oriented in concepts like Cache Memory, Pipeline Architecture, and in the design of Single Purpose Processors. This course facilitates the student with the knowledge of various components needed to design an embedded system meeting the requirement specification. The course also deals with case studies where differentprocessor architectures are used to design embedded systems with an emphasis on the VLSI perspective. These case studies enable the student to do design selection and design comparisons based on various design optimization parameters and requirement specifications.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course, the student will be able to

CO 1	Understand and apply various aspects of hardware and software architectures in embedded system design.
CO 2	Differentiate various embedded system technologies and their implications on embedded system design.
CO 3	Design, analyse and optimise different single-purpose processor architectures.
CO 4	Evaluate and analyse different cache memory configurations. Distinguish various communication protocols and interfaces.
CO 5	Assess different embedded system case studies.
CO 6	Design an embedded system by identifying the best processor architecture based on the requirement specifications and design optimization matrices.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3	2	1	2	1	2		1	1	2
CO 4	2	1	2	2	1		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation (%)	End Semester Examination (%)
Apply	20	20
Analyse	30	30
Evaluate	30	30
Create	20	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Sl No	Pattern	Marks	Remarks
1.	Preparing a review article based on peer-reviewed original publications	15	Minimum 10 publications shall be referred.
2.	Course-based task / Seminar / Data collection and interpretation	15	
3.	Test paper	10	1 No Test paper shall include a minimum of 80% of the syllabus

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Syllabus

Module	Contents	Hours
1	**Introduction to Embedded Systems:** Introduction, common characteristics and categories of embedded systems, general requirements of embedded systems, design metrics and its optimization, embedded system development process, an overview of embedded system architecture, hardware architecture, software architecture, hardware- software co-design, computational models, introduction to unified modelling language, hardware-software trade-offs.	8
2	**General-purpose Processors & Application Specific Instruction-Set Processors:** Embedded System Technologies, General-purpose processors, pipeline, pipeline hazards, superscalar and VLIW architectures, Application Specific Instruction-Set Processors (ASIP's). Selecting a Microprocessor / General Purpose Processor.	8
3	**Single Purpose Processors (Standard & Custom):** **Standard SPP:** Timers, Counters, Watchdog Timer, Real-Time Clock, UART, Pulse Width Modulator, LCD Controller, Keypad Controller. **Custom SPP:** RT- level Custom Single purpose Processor Design, Optimizing the original program, Optimizing the FSMD, Optimizing the datapath, and optimizing the FSM.	8
4	**Memory & Communication Protocols:** **Memory:** Memory classification, ROM, RAM, Memory hierarchy, Cache, Cache Mapping, Cache write policy, Cache update policy, Cache Coherency. **Communication Protocols:** Serial - RS232, RS422/RS485, I2C, SPI, USB, Ethernet, CAN. Parallel - PCI bus, AMBA bus. Wireless - Bluetooth, IEEE 802.11, LoRaWAN.	8

5	**Case Study – Digital Camera & Control System:** **Digital Camera:** User's perspective, designer's perspective, specification, informal functional specification, non-functional specification, executable specification. Design, Implementation, and Comparison - microcontroller- based implementation, fixed point FDCT implementation, hardware FDCT implementation. **Control System:** Open-loop and closed-loop control systems, an open-looped automobile cruise controller, a closed-loop automobile cruise-controller, general control systems and PID controllers, practical issues related to computer-based control, and benefits of computer-based control implementations.	**8**

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

Marks: 60 marks **Duration: 2.5 hours**

PART A

Answer all Questions: 5 marks each – 5 x 5 = 25 marks

1. Write a short note on five common characteristics of Embedded Systems with examples.
2. What is pipelining? "Increasing the number of pipelines stages improves the processor performance" Justify the statement with example.
3. Briefly explain about RTC with a neat diagram. Explain about the power backup scheme implemented with RTC. Why 32.768 KHz is given as the standard frequency for RTC clock?
4. List down any two signal component of I2C bus. Briefly explain the I2C arbitration process with neat diagram.
5. In the context of digital camera what is informal functional specification and what is refined functional specification? Considering a digital camera discuss on the statement "a design metric can be both constrained and optimized".

PART B

Answer

Answer any 5 Questions: 7 marks each – 5 x 7 = 35 marks

6. Analyse the hardware architecture of an embedded system with a neat diagram.
7. What are Pipeline Hazards? Categorise various Pipeline Hazard and discusson methods to solve them.
8. Develop an algorithm, draw the state diagram, and design the datapath of a custom single purpose processor to determine the sum of digits of a number. Propose the block diagram and FSMD of its controller.
9.

a. A 64 bit microprocessor running at 100 MHz speed is designed with an L1 cache which interacts with a DRAM of 50 cycles read time. Four design suggestionsare listed below. Calculate the Average Memory Access Time, identify the best design and analyze the same. **(4 marks)**

i. L1 cache,1K size, miss rate = 20%, hit time = 3 cycles
ii. L1 cache,2K size, miss rate = 15%, hit time = 4 cycles
iii. L1 cache,4K size, miss rate = 10%, hit time = 5 cycles

b. Consider a cache with 4 memory locations with LRU replacement policy. Memory blocks 5, 3, 20, 45, 3, 5, 4, 20, 4, 45, 23 are requested by processor. What will be the status of cache after this operation? **(3 marks)**

10. Analyse the closed loop cruise control system with a neat diagram andcompare the Proportional controller with Proportional Integral controller.

11. Develop an algorithm, draw the state diagram, and design the datapath of a custom single purpose processor to implement pow (x, n) function. Propose the block diagram and FSMD of its controller.

12.

a. Consider a system with 3 level caches. Access times of Level 1 cache, Level 2 cache, Level 3 cache and main memory are 1 ns, 15ns, 30ns, and 500 ns, respectively. The hit rates of L1, L2 and L3 caches are 0.85, 0.92 and 0.95, respectively. What is the average access time of the system neglecting the miss penalties? **(4 marks)**

b. The floating point operations of a processor need to be enhanced by introducing a new advanced FPU unit. Let the new FPU is 10 times faster on floating point computations than the original processor. Assuming a program has 40% floating point operations, what is the overall speedup gained by incorporatingthe enhancement? **(3 marks)**

Syllabus and Course Plan (For 3 credit courses, the content can be for 40 hrs andfor 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to Embedded Systems**	
1.1	Introduction, Common Characteristics, and Categories of embedded systems.	1
1.2	General requirements of embedded systems – performance, size, reliability and ruggedness, cost-effectiveness, power consumption, user interfaces, software updating capability.	1
1.3	Design challenges, design metrics, and optimization.	1
1.4	Embedded System Development Process, Overview of Embedded System Architecture.	1
1.5	Hardware Architecture – CPU, memory, input devices, output devices, communication interfaces, application specific circuitry.	1

1.6	PCB concepts: PCB, Multilayer PCB, stack up, track, via, signal integrity basics (impedance, reflection, ringing, cross talk, simultaneous switching noise), component packages (through-hole and SMT), PCB assembly (manual vs automatic), and PCB testing.	1
1.7	Software Architecture, challenges, and issues related to embedded software development, fundamental issues in hardware software co-design,	1
1.8	Computational models in Embedded Design, Introduction to Unified Modeling Language, hardware-software Trade-offs.	1
2	**General-purpose Processors & Application Specific Instruction-Set Processors**	
2.1	Embedded System Technologies: Processor Technology, IC Technology, and Design Technology.	2
2.2	General-purpose Processors: Basic architecture, Datapath, Control unit	1
2.3	Pipelining, Standard 5 stage pipeline, Pipeline Hazards.	3
2.4	Superscalar and VLIW architectures.	1
2.5	Application Specific Instruction-Set Processors (ASIP's): Microcontrollers, DSP, Less- General ASIP environments. Selectinga Microprocessor / General Purpose Processor - performance parameters, Amdahl's law, and benchmark.	1
3	**Single Purpose Processors (Standard & Custom)**	
3.1	Standard SPP: Timers, Counters, Watchdog Timer, Real-Time Clock.	1
3.2	Standard SPP: UART, Pulse Width Modulator, LCD Controller, Keypad Controller.	1
3.3	Custom SPP: RT- level Custom Single purpose Processor Design	5
3.4	Custom SPP: Optimizing the original program, optimizing the FSMD, optimizing the datapath, and optimizing the FSM.	1
4	**Memory & Communication Protocols**	
4.1	Memory: Memory classification, ROM, RAM, Memory hierarchy, Cache, Cache Mapping, Cache write policy, Cache update policy.	3
4.2	Serial: RS232, I2C (including arbitration), SPI, USB, Ethernet, CAN.	3
4.3	Parallel: PCI bus, AMBA bus.	1
4.4	Wireless: Bluetooth, IEEE 802.11, LoRaWAN	1
5	**Case Study – Digital Camera & Control System**	
5.1	Digital Camera: User's perspective, Designer's perspective, Specification, Informal Functional specification, Non-functional specification. Executable specification.	1
5.2	Digital Camera: Design, Implementation, and Comparison - microcontroller based implementation, fixed point FDCT implementation, hardware FDCT implementation.	3
5.3	Control System: Open-loop and closed loop control systems, an open-looped automobile cruise controller, a closed-loop automobile cruise-controller, and General control systems (P,PI, PD, and PID controllers).	3

5.4	Practical Issues Related to computer-based control, Benefits of computer-based control Implementations.	1

Reference Books

1. Frank Vahid and Tony Givargis, Embedded System Design-A Unified Hardware/Software Introduction", John Wiley & Sons, 2002.
2. William Stallings, Computer Organization and Architecture : Designing for Performance, Pearson Education 2016
3. Marilyn Wolf, Computer as Components Principles of Embedded Computing System Design, Elsevier, 2012
4. Steve Heath, Butterworth Heinemann, "Embedded System Design." Newnes, 2nd edition (December 25, 2002)
5. Jorgen Staunstrup, Wayne Wolf (editors), Hardware/Software Co-Design: Principles and Practice, Springer, 1997
6. Gajski and Vahid, "Specification and Design of Embedded systems", Prentice Hall.
7. Rajkamal, "Embedded systems: Architecture, Programming and Design",TMH, 2012.
8. Shibu K.V.," Introduction to Embedded Systems, Tata McGraw Hill Education Private Limited, 2010.
9. Alexandru Forrai, Embedded Control System Design: A Model Based Approach, Springer, 2013
10. Alberto Sangiovanni-Vincentelli, Haibo Zeng • Marco Di Natale, PeterMarwedel, Embedded Systems Development : From Functional Models to Implementations, Springer, 2014
11. Bruce Powel Douglass, Real-Time UML Workshop for Embedded System, Elsevier; First edition (1 January 2010)
12. Kraig Mitzner, Complete PCB Design Using OrCAD Capture and PCB Editor, Elsevier Inc, 2009

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC039	MULTIRATE SIGNAL PROCESSING AND WAVELETS	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: This course will help to understand about the concept of multi rate signal processing and different wavelets used for signal processing. It introduces the design with filter banks.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	To understand the concepts of sampling rate conversions, Decimation and Interpolation.
CO 2	To describe basic sampling rate conversion algorithms.
CO 3	To draw and describe different kinds of interpolators and decimators.
CO 4	To analyse how the interpolated FIR filter works.
CO 5	To understand the basic concepts of wavelet bases and time-frequency analysis.
CO 6	To design a basic wavelet filter bank.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	-	-	3	-	-	1	-	1	
CO 2	3	-	2	3	-	-	-	2	2
CO 3	1	-	-	3	-	2	-	2	2
CO 4	3	-	3	-	2	1	-	2	1
CO 5	2	-	3	1	-	-	-	1	2
CO 6	1	-	3	3	2	-	-	1	2

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40
Analyse	40
Evaluate	20
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marksTest

paper, 1 No.: 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION

VLSI Design and Signal Processing

MULTIRATE AND WAVELETS

Max. Marks : 60 Duration: 2.5 Hours

PART A

Answer all questions (5 x 5=25 Marks)

1. What is subband coding?
2. List out the steps involved in multistage sampling rate converter design.
3. What are polyphase filters?
4. Write notes on time-frequency analysis.
5. How are bi-orthogonal wavelets different from orthogonal wavelet systems?

PART B

Answer ONE question from each module (5 x 7=35 Marks)

6. Draw the block diagram of a 2-channel analysis and synthesis filter bank.
7. With the required expressions, illustrate how Reconstruction of the signaltakes place in QMF Bank.
8. Analyze Cosine modulated QMF bank Systems with a neat block diagram.
9. Discuss in detail, the dyadic muti-resolution analysis using Haar wavelet.
10. Explain how wavelets are used to achieve signal compression?
11. Discuss about coefficient sensitivity effects, dynamic range and scaling in Perfect Reconstruction Filter banks.
12. In detail, explain the design steps in an orthogonal wavelet system.

Syllabus

Module 1: Basic multirate operations, Interconnection of building blocks, Polyphase representation, Multistage implementation, Applications of multirate systems, Special filters and filter banks.

Module 2: Perfect reconstruction filter banks – Introduction, Lossless transfermatrices, 2-channel FIR QMF banks, 2-channel QMF lattice, M – channel FIR filter banks.

Module 3: FIR filter banks - Introduction, necessary conditions, Lattice structure for linear phase FIR PR banks, Synthesis of linear phase FIR PR QMF Lattice, Pseudo QMF banks, Design of the pseudo QMF bank, Efficient polyphase structure, Cosine modulated perfect reconstruction system.

Module 4: Introduction to Fourier transform and Short time Fourier transform, Time-frequency analysis, Bases of time frequency: orthogonal, Filter banks, Multi resolution formulation, Continuous Wavelet Transform Continuous wavelet transform (CWT), Time and frequency resolution of the continuous wavelet transform.

Module 5: Discrete wavelet transform and filter banks - Orthogonal and biorthogonal two-channel filter banks, Design of two-channel filter banks, Non- linear approximation in the Wavelet domain, multi resolution analysis, Applicationsof wavelets - Signal and Image compression, Wavelet based signal de-noising and energy compaction.

Course Plan

No	Topic	No. of Lectures
1	**Module - 1**	
1.1	Basic multirate operations, Interconnection of building blocks	2
1.2	Polyphase representation, Multistage implementation	3
1.3	Applications of multirate systems, Special filters and filter banks.	3
2	**Module - 2**	
2.1	Perfect reconstruction filter banks – Introduction, Lossless transfer matrices	2
2.2	2-channel FIR QMF banks, 2-channel QMF lattice	3
2.3	M – channel FIR filter banks	3
3	**Module - 3**	
3.1	FIR filter banks - Introduction, necessary conditions, Lattice structure for linear phase FIR PR banks	2

3.2	Synthesis of linear phase FIR PR QMF Lattice, Pseudo QMF banks, Design of the pseudo QMF bank	3
3.3	Efficient polyphase structure, Cosine modulated perfect reconstruction system.	2
4	**Module - 4**	
4.1	Introduction to Fourier transform and Short time Fourier transform, Time-frequency analysis.	2
4.2	Bases of time frequency: orthogonal, Filter banks, Multi resolution formulation.	2
4.3	Continuous Wavelet Transform Continuous wavelet transform (CWT), Time and frequency resolution of the continuous wavelet transform.	2
5	**Module - 5**	
5.1	Discrete wavelet transform and filter banks - Orthogonal and biorthogonal two-channel filter banks	3
5.2	Design of two-channel filter banks, Non-linear approximation in the Wavelet domain, multi resolution analysis	3
5.3	Applications of wavelets - Signal and Image compression, Wavelet based signal de-noising and energy compaction	3

Reference Books

1. P.P.Vaidyanathan , PTR Prentice Hall, Englewood Cliffs , New Jersey,Multirate System and Filter Banks.
2. N.J.Fliege , John Wiley and Sons, Multirate Digital Signal Processing.
3. A Wavelet Tour of Signal Processing, 2nd edition, S. Mallat, Academic Press, 1999.
4. Insight into wavelets from theory to practice, K P Soman and KL Ramachandran, PHI, 2008.

SEMESTER II

PROGRAM ELECTIVE IV

SLOT	SL NO	COURSE CODE	COURSE NAME	L-T-P	HOURS	CREDIT
D	1	24SJ2EEC040	LOW POWER VLSI	3-0-0	3	3
	2	24SJ2EEC041	VLSI SYSTEM TESTING	3-0-0	3	3
	3	24SJ2EEC042	HIGH SPEED DIGITAL DESIGN	3-0-0	3	3
	4	24SJ2EEC021	DEEP LEARNING	3-0-0	3	3
	5	24SJ2EEC044	STATIC TIMING ANALYSIS	3-0-0	3	3
	6	24SJ2EEC045	SIGNAL COMPRESSION	3-0-0	3	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC040	LOW POWER VLSI	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble: This course aims to develop students a good knowledge on designing low power VLSI circuits by estimating and analysing power dissipation using different methodologies and thereby implementing low power design methodologies in different levels of design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design chips for battery powered systems and high performance circuits not exceeding power limits and examine analyze power dissipation using simulation.
CO 2	Examine the power dissipation using power analysis like probabilistictechniques and to understand power dissipation in clock distribution for accurate working of circuit.
CO 3	Design low power circuits at circuit and logic level.
CO 4	Analyze performance management techniques and low power memory design techniques.
CO 5	Understand advanced topics like adiabatic switching.

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation anddevelopment work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40
Analyse	40
Evaluate	20
Create	-

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed Original publications (minimum10 publications shall be referred) : 15 marks

Course based task/Seminar/Micro project : 15 marksTest

paper 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

End Semester Examination: 60 marks

The end semester examination will be conducted by the respective college.

There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION,DEC 2022

Branch: Electronics & Communication

Course Code & Name: 24SJ2EEC040 LOW POWER VLSI

	Answer *All Questions(5 Marks each)*
1.	Illustrate short circuit current variation in CMOS circuits with loadcapacitance and input signal slope.
2.	Explain different types of clock driving scheme
3.	Illustrate how the network restructuring helps in leakage power reduction.
4.	Discuss the concepts and operation of 6T SRAM memory cell with allnecessary diagrams and tables.
5.	Discuss fully adiabatic system and formulate E_{total}
	Answer *Any 5 Questions(7 Marks each)*
6.	Using Gate level Capacitance estimation, analyze the gate level power dissipation of a circuit.
7	Discuss about charging and discharging capacitance of CMOS device. Derive an expression for power dissipation.
8.	Derive an expression for total transition density and explain gate levelpower analysis using transition density
9.	Using necessary mathematical equations, explain how you will relate the static probability of a digital signal to switching frequency.
10.	Illustrate how the transistor sizing helps in leakage power reduction.
11.	Explain how switching activities can be reduced in CMOS digital systems
12.	Explain adiabatic amplification with a neat diagram. Derive an expression for E_{load}

Module 1

Need for low power VLSI chips and Simulation Power analysis: Introduction - Need for low power VLSI, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, Basic principles of low power design, **Simulation Power analysis:** SPICE circuit simulation, **Gate level logic simulation** - capacitive power estimation, static state power, gate level capacitance estimation

Module 2

Probabilistic Power analysis and Low power Clock Distribution: Probabilistic power analysis: Random logic signals, Probability & frequency, Probabilistic power analysis techniques, **Low power Clock Distribution:** Power Dissipation In Clock Distribution, Single Driver Vs Distributed Buffers

Module 3

Low Power Design- Circuit and Logic level: Circuit level: Transistor & Gate sizing, Network restructuring & reorganization, Special Latches & flip-flops, **Logic level:** Gate Reorganization, Signal Gating, Logic Encoding

Module 4

Low power Architecture & Systems: Power & Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, **Low Power Memory Design:** Low power static RAM – organization of static RAM, MOS static RAM cell, Banked organization of SRAMs

Module 5

Adiabatic switching, Adiabatic charging, Adiabatic amplification, one stage and two stage adiabatic buffer in conventional system, fully adiabatic sequential circuits, stepwise charging, pulsed power supplies.

Course Plan

No	Topic	No. of Lectures
1	**Need for low power VLSI chips and Simulation Power analysis:**	
1.1	Introduction - Need for low power VLSI chips	1
1.2	Charging and Discharging capacitance	1
1.3	Short Circuit current in CMOS circuit	1
1.4	CMOS leakage current, Static current	1
1.5	Basic principles of low power design	1
1.6	**Simulation Power analysis:**	
1.6.1	SPICE circuit simulation	1
1.6.2	**Gate level logic simulation** - Capacitive power estimation, Static state power, Gate level capacitance estimation	2

2.	**Probabilistic Power analysis and Low power Clock Distribution:**	
	Probabilistic power analysis:	
2.1	Random logic signals	1
2.2	Probability & frequency	1
2.3	Probabilistic power analysis techniques	3
	Low power Clock Distribution:	
2.4	Power Dissipation In Clock Distribution	1
2.5	Single Driver Vs Distributed Buffers	2
3	**Low Power Design- Circuit and Logic level**	
	Circuit level:	
3.1	Transistor & Gate sizing	2
3.2	Network restructuring & reorganization	1
3.3	Special Latches & flip-flops	2
	Logic level	
3.4	Gate Reorganization	1
3.5	Signal Gating	1
3.6	Logic Encoding	1
4	**Low power Architecture & Systems:**	
4.1	Power & Performance Management	1
4.2	Switching Activity Reduction	2
4.3	Parallel Architecture With Voltage Reduction	2
4.4	**Low Power Memory Design**	
4.4.1	Low power static RAM – Organization of static RAM	1
4.4.2	MOS static RAM cell, Banked organization of SRAMs	2
5	**Adiabatic switching**	
5.1	Adiabatic switching – Adiabatic charging	2
5.2	Adiabatic amplification	1
5.3	One stage and Two stage adiabatic buffer in conventional system	2
5.4	Fully Adiabatic Sequential Circuits	1
5.5	Stepwise Charging	1
5.6	Pulsed Power Supplies.	1

Reference Books

1. Rabaey, Pedram, "Low power design methodologies" Springer Science & Business Media, 2012.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.
4. Anatha P Chandrakasan, Robert W Brodersen, "Low power digital CMOS Design", Kluwer Academic.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC041	VLSI SYSTEM TESTING	PROGRAMM EELECTIVE 4	3	0	0	3

Preamble: This course aims to provide a strong base in digital VLSI Testing. In this course, different fault models and methods for test generation and application are discussed. Syllabus covers concepts of Scan architecture and BIST. The course equips the learner to design a test environment.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Interpret fault models and to create collapsed fault list.
CO 2	Develop simulators and to calculate SCOAP measures
CO 3	Generate test vectors for combinational and sequential circuits
CO 4	Generate test vectors for memory faults and delay faults
CO 5	Design scan architecture and pattern generators

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1
CO 5		1	2	2	2		1	1	2

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40
Analyse	50
Evaluate	10
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marks
Test paper, 1 No.: 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE: **PAGES: 2**

Reg No:_____ **Name:____**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ1EEC041 Course

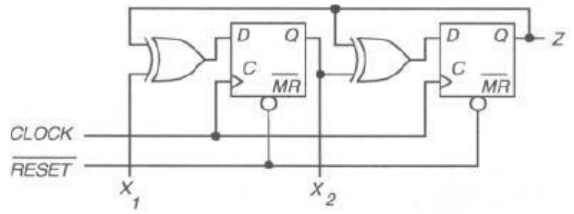
Name: VLSI System Testing

Max. Marks: 60 **Duration: 2.5 Hours**

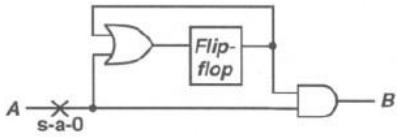
PART A

Answer all Questions. Each question carries 5 Marks

1. What is the significance of fault equivalence set? Illustrate with an example.
2. Calculate the sequential SCOAP testability measures for the circuit shown below. Assume synchronous clock.



3. Derive a test for this fault using nine valued logic.



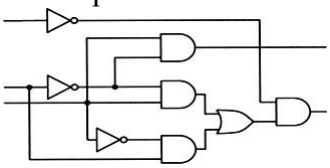
4. What are the robust path delay sensitization conditions for NAND gate and OR gate?
5. For a circuit with 1,00,000 gates and 2,000 flipflops, connected in a single scan chain, what is the gate overhead?

(5x5=25 Marks)

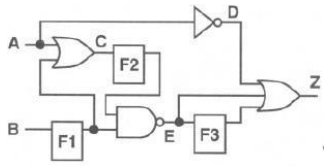
PART B

Answer any 5 questions. Each question carries 7 marks

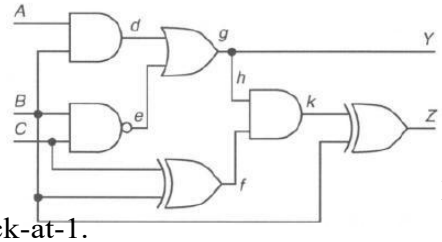
6. (a) What is Check Point Theorem?
   (b) Identify the check points of the following circuit.



7. Calculate the combinational SCOAP values for the circuit shown in 6.(b).
8. Derive a test pattern to detect D Stuck-at-0.



9. Consider the circuit shown below. Use D-Algorithm to derive a test vector forh Stuck-at-0.



10. Does MATS algorithm (k-at faults? Justify for cases, Stuck-at-0 and Stuck-at-1.
11. For the characteristic equation $x^3 + x^2 + x + 1$,
    (a) draw standard LFSR
    (b) derive companion matrix Ts for the standard LFSR
12. With relevant block diagrams and waveforms, explain Enhanced-Scan Test.

(5x7=35 Marks)

Syllabus

Module 1 Fault Models and Fault Collapsing

Role of Testing, Structural Testing, Fault Modeling, Glossary of Fault Models, Fault Equivalence, Fault Collapsing, Fault Dominance, Check Point Theorem

Module 2 Simulation and Testability Measures

True Value Simulator, False Simulator, Algorithms for True Value Simulation – Compiled Code Simulation, Event Driven Simulation, Algorithms for Fault Simulation – Serial Fault Simulation, Parallel Fault Simulation, Combinational SCOAP Measures, Sequential SCOAP Measures

Module 3 Circuit Test Generation

ATPG Algebras – Roth's 5 Valued Algebra, Muth's 9 Valued Algebra, AlgorithmTypes, Redundancy Identification, Combinational ATPG Algorithms – D-Algorithm, PODEM, Sequential ATPG Algorithm – Time Frame Expansion Method

Module 4 Memory Test and Delay Test

Memory Faults, Fault Manifestations, Failure Mechanisms, March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects, Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies

Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads ofScan Design, Partial-Scan Design, Variations of Scan, Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR, BIST Response Compaction using LFSR, Multiple Input Signature Register

Course Plan

No	Topic	No. of Lectures
1	**Fault Models and Fault Collapsing**	
1.1	Role of Testing	1
1.2	Structural Testing, Fault Modeling, Glossary of Fault Models	3
1.3	Fault Equivalence, Fault Collapsing, Fault Dominance, Check Point Theorem	4
2	**Simulation and Testability Measures**	
2.1	True Value Simulator, False Simulator, Algorithms for True Value Simulation – Compiled Code Simulation, Event Driven Simulation, Algorithms for Fault Simulation – Serial Fault Simulation, Parallel Fault Simulation	4
2.2	Combinational SCOAP Measures, Sequential SCOAP Measures	4
3	**Circuit Test Generation**	
3.1	ATPG Algebras – Roth's 5 Valued Algebra, Muth's 9 Valued Algebra, Algorithm Types, Redundancy Identification	2
3.2	Combinational ATPG Algorithms – D-Algorithm, PODEM	3
3.3	Sequential ATPG Algorithm – Time Frame Expansion Method	2
4	**Memory Test and Delay Test**	
4.1	Memory Faults, Fault Manifestations, Failure Mechanisms	1
4.2	March Test Notations, Fault Modeling, Reduced Functional Faults, Relation between Fault Models and Physical Defects	4
4.3	Delay Test Problem, Test Generation for Combinational Circuits, Transition Faults, Delay Test Methodologies	4
5	**DFT and BIST**	
5.1	Ad-Hoc DFT Methods, Scan Design Rules, Tests for Scan Circuits, Overheads of Scan Design	2
5.2	Partial-Scan Design, Variations of Scan	1
5.3	Random Logic BIST – BIST Process, BIST Implementations, Pseudo Random Pattern Generation using Standard LFSR, using Modular LFSR	2
5.4	BIST Response Compaction using LFSR, Multiple Input Signature Register	2

Reference Books

1. Viswani D Agarwal and Michael L Bushnell, "Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits", Springer, 2000.

2. M. Abramovici, M A Breuer and A D Friedman, "Digital systems Testing and Testable Design", IEEE Press, 1994

3. Niraj Jha and Sanjeep K Gupta, "Testing of Digital Systems", Cambridge Institute Press, 2003.

4. L-T Wang, C-W Wu, and X. Wen "VLSI Test Principles and Architectures: Design for Testability", Academic Press, 2006

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC042	HIGH SPEED DIGITAL DESIGN	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble:

- · To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

Course Outcomes: The COs shown are only indicative. For each course, there canbe 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Adapt to go far into the world of high speed digital design.
CO 2	Describe the wire model inventory, noise, signaling, and synchronization ideas related to high-speed design.
CO 3	Understanding the trade-offs between noise immunity, power, speed, andother factors can help you build high-speed systems and other linked domains.
CO 4	To learn troubleshooting clock problems in VLSI designs

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1		1	2	2	2		1	2	2
CO 2		1	2	2	2		1	2	2
CO 3		1	2	2	2		1	1	2
CO 4		1	2	2	2		1	1	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	35
Analyse	30
Evaluate	25
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course-based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 No. : 10 marks

Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, witha minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)
M.TECH DEGREE EXAMINATION, JUNE 2022

DEPARTMENT OF ELECTRONICS AND

COMMUNICATIONVLSI & EMBEDDED SYSTEMS/

EMBEDDED SYSTEMS

Max. Marks: 60 **Duration: 2.5 Hrs**

PART – A **25 marks**

(Answer All Questions. All Questions Carry Equal Marks)

1. Describe the electrical properties of wires.
2. Differentiate bipolar versus unipolar signalling. Draw the clocked RZ andclocked NRZ wave forms for the data 101100
3. Discuss the effect of cross talk in power supply network.
4. Write about simultaneous signalling
5. Discuss the importance of set up time and hold time with help of neatdiagrams.

PART – B

Answer All Questions (7 Marks Each)

6. Discuss the importance of knee frequency in the performance of high-speed digital circuits (7)

OR

7 A 20m-longless transmission line with Zo=75Ω operating at 1 MHz is terminated with a load Z_L=100+j150Ω, find (7)

a. The reflection coefficient
b. The standing wave ratio S

8. write a short note on area bonding, IR dropping, on chip bypass capacitors (7)

OR

9. Discuss the different types of power supply isolation techniques. (7)

10. a. Discuss the noise sources in digital system (3)

b.discuss the importance of noise budgeting and inter symbol interference terms inciruit design (4)

OR

11. Explain in detail different power supply noises. (7)

12. Explain in detail signalling over lumped transmission line (7)

OR

13 Explain simultaneous and bidirectional signalling (7)

14. List the different on chip clock distribution networks? Explain any one of themwith relevant diagrams. (7)

OR

15. Explain the term metastability and synchronization failures (7)

Syllabus and Course Plan

(For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in the third semester can have contentfor 30 hours).

No	Topic	No. of Lectures
	HIGH SPEED DIGITAL DESIGN	
1	**Module 1**	
1.1	Frequency, time and distance, Knee Frequency and its significance, Propagation Delay, Capacitance and Inductance Effects	3
1.2	High speed properties of logical gates, Speed and power. Geometry and Electrical properties of wires, Electrical model of wires.	3
1.3	Lattice Diagram Analysis of Transmission Lines, Simpleand Special Transmission Lines.	2
2	**Module 2**	
2.1	Power supply network, Local power regulation, IR drops, Area bonding,	2
2.2	On chip bypass capacitors, Bypass Capacitor Design	2

2.3	Symbiotic bypass capacitors	1
2.4	Power supply isolation	1
3	**Module 3**	
3.1	Power supply Noise	2
3.2	Cross talk, Noise budgeting and SNR	2
3.3	Signal Interference, inter-symbol Interference	2
3.4	Noise sources in digital system , Statistical Analysis.	1
4	**Module 4**	
4.1	Signalling modes for transmission lines	2
4.2	signalling over lumped transmission media	2
4.3	signalling over RC interconnects, driving lossy LC lines	2
4.4	simultaneous bi-directional Signalling	2
4.5	Terminator circuits. PLL and DLL based clock aligners.	2
5	**Module 5**	
5.1	Timing fundamentals, Timing properties of clocked storage elements,.	1
5.2	signals and events, Open loop Timing, level sensitive clocking	1
5.3	Pipeline Timing, Closed loop Timing.	1
5.4	Synchronisation failure and metastability,	2
5.5	probability of synchronization failure Hierarchy of synchronizer design – delay line,	2
5.6	2-register and FIFO mesochronous synchronizers	1

Reference Books

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbookof Black Magic by",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006

2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices" by , Wiley , 2007

3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006

4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC021	DEEP LEARNING	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: This course provides an introduction to key concept in deep learning and equip students with knowledge required to develop best deep learning solutions for real world problems in domains such as computer vision, natural language processing etc.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Demonstrate the uses and limitations of fully connected neural networks
CO 2	Compare different CNN networks for classification and detection in terms of architecture, performance and computational requirements
CO 3	Develop a convolutional neural network for a real-world application
CO 4	Apply regularization and optimization techniques in CNN training
CO 5	Demonstrate the use of RNNS and LSTM for analysing sequential data
CO 6	Apply the concepts of attention models, transformers and generative models

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3								
CO 2	3							3	3
CO 3	3		3	3	3				
CO 4	3								
CO 5	3							3	3
CO 6	3		3	3				3	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	60%
Analyse	40%
Evaluate	
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Course project: 15 marks
Course based task/Seminar/Quiz: 15 marksTest paper, 1 no.: 10 marks

End Semester Examination Pattern:

60 Marks
Part A: 5×5 Marks
Part B: 5×7 Marks

Course Level Assessment Questions

Course Outcome 1 (CO1):

1. Suppose you have a 3-dimensional input $x = (x_1, x_2, x_3) = (2, 2, 1)$ fully connected with weights (0.5, 0.3, 0.2) to one neuron which is in the hidden layer with sigmoid activation function. Calculate the output of the hidden layer neuron.
2. Consider the case of the XOR function in which points {(0, 0), (1, 1)} belong to one class, and {(1, 0), (0, 1)} belong to the other class. Design a multilayer perceptronfor this binary classification problem.

Course Outcome 2 (CO2)

1. Implement AlexNet, VGG Net, ResNet and Inception Net for a classification problem. Compare and contrast the performance in terms of accuracy and computational requirements.
2. Implement RCNN, Fast RCNN, Faster RCNN, YOLO and Mask RCNN for detection problem. Compare and contrast the performance in terms of accuracy and computational requirements.

Course Outcome 3(CO3):

3. Draw and explain the architecture of convolutional neural networks.
4. You are given a classification problem to classify the handwritten digits. Suggesta learning algorithm with its architecture, an objective function, and an optimization routine, along with how input and output will be prepared for the classifier

Course Outcome 4 (CO4):

1. Explain how L2 regularization improves the performance of deep feed forwardneural networks.
2. Explain the use of data augmentation and dropouts

Course Outcome 5 (CO5):

1. Illustrate the workings of the RNN with an example of a single sequence definedon a vocabulary of four words
2. Draw and explain the architecture of LSTM.
3. List the differences between LSTM and GRU

Course Outcome 6 (CO6):

1. Explain the use of transformers for image recognition
2. Explain the basic principle and architecture of generative adversarial network

Model Question paper

PART A

1 There is huge gap between training accuracy and testing accuracy, while training a particular machine learning model. What might be the reason. Suggest possible methods of overcoming it 5

2 Draw the block diagram of a naïve inception block. What is the disadvantage of this block? Explain how adding 1x1 convolution helps toovercome the difficulty. 5

3 Consider a Convolutional Neural Network having three different convolutional layers in its architecture as 5

Layer-1	Filter Size – 3×3, Number of Filters – 10, Stride – 1, Padding – 0
Layer-2	Filter Size – 5×5, Number of Filters – 20, Stride – 2, Padding – 0
Layer-3	Filter Size – 5×5 , Number of Filters – 40, Stride – 2, Padding – 0

If we give a 51×51 RGB image as input to the network, then determinethe dimension of the vector after passing through layer 3 in the architecture.

4 You have a dataset D1 with 1 million labelled training examples for classification, and dataset D2 with 100 labelled training examples. Your friend trains a model from scratch on dataset D2. You decide to train on D1, and then apply transfer learning to train on D2. State one problem your friend is likely to find with his approach. How does your approach address this problem? 5

5 Differentiate between soft attention and hard attention. 5

PART B

6 Astronomers are using a linear classifier to classify long exposed CCD images into star, nebula and galaxy. The predicted scores of this linear classifier, during one particular iteration of training is given below 7

Class	Test Image		
	Star	Nebula	galaxy
Star	3.2	1.3	2.2
Nebula	5.1	4.9	2.5
Galaxy	-1.7	2	-3.1

Calculate the softmax loss for Nebula. Find minimum and maximum softmax loss, if there are C classes.

7 Draw the computational graph and calculate the analytical gradients at each node for the following function 7

$$ff(w,x) = \frac{1}{1+e^{-(w0x0+w1x1+w2)}}$$

where $w_0 = 2,\ w_1 = -3, w_2 = -3,\ x_0 = -1,\ x_1 = -2$

8 Consider a CNN implemented with following arrangement. 7

Input 128x128x3

Conv 4- 10, stride 2, pad 0

Conv 9-10,stride 2, pad 2

Pool 2 stride 2, pad 0

Conv 3-5 stride 2, pad 0
FC 5

FC-N denotes fully connected layer with N neuron outputs. Conv M-N indicates convolution layer of size MxMxD, with M filters and D activation volume of previous layer. Pool 2 indicates 2x2 maxpooling layer. Find activation volume and number of parameters at each layer.

9	Write disadvantages of SGD. Explain how ADAM overcome it.	7
10	Imagine you were asked to write a poem in the writing style of John Keats. What kind of network will you use? Draw and explain the structure of identified network with equations.	7
11	You were asked to design an object detection frame work to be used in Google's autonomous car Waymo. The designed framework should be able to detect and identify multiple objects (pedestrians, other vehicles etc.) from images obtained from the camera feed of Waymo. Draw and explain the general structure of the network. Justify your answer.	7
12	Design a network to generate your photo in the style of Leonardo DaVinci'sMonalisa.	7

SYLLABUS

MODUE 1: Introduction to Machine Learning

Introduction: Supervised Vs. Unsupervised Learning, Classification Vs. Regression,Machine Learning Vs. Deep Learning

Machine Learning System Design: Data-driven Approach, Datasets: Training,Testing and Validation Sets, Over fitting and Under fitting, Hyper parameters, K-nearestneighbour classification.

Linear classification: Loss function, Multiclass SVM,Softmax classifier. Optimization, Numeric andAnalytic gradients.

MODULE 2: Neural Networks

Deep feedforward networks/ Multilayer perception: Perceptron, activation functions, Example: Learning XOR, Architecture of deep neural network

Back propagation, Gradient-Based Learning.

Convolutional Neural Networks: Convolution, Pooling Layers, spatialarrangement, layer patterns, layer sizing patterns.

MODULE 3: Training Neural Networks

Initialization, batch normalization, Hyper parameter optimization. Optimization algorithms: SGD, Momentum, Adagrad, RMS Prop, Adam

Regularization methods: L1 and L2 regularization, Early stopping, drop outs, ensembles, data augmentation, Update rules, transfer learning

MODULE 4: CNN architectures

AlexNet, VGG Net, ResNet, Inception Net

Object Detection: RCNN, Fast RCNN, Faster RCNN, YOLO, Mask RCNN

Recurrent Neural Networks: RNN, Bidirectional RNN, LSTM, GRU

MODULE 5: Attention Models, Transformers and Generative Models

Attention: Multimodal attention, Self-Attention

Transformers: BERT and vision transformer

Autoencoders, Variational auto encoders, Generative Adversarial Network

Course Plan

No	Topic	No. of Lectures
1	**Introduction to Machine Learning**	
1.1	Introduction: Supervised Vs. Unsupervised Learning, Classification Vs. Regression, Machine Learning Vs. Deep Learning	1
1.2	Machine Learning System Design: Data-driven Approach,Datasets: Training, Testing and Validation Sets, Over fitting and Under fitting, Hyper parameters, K-nearestneighbour classification	3
1.3	Linear classification: Loss function, Multiclass SVM, Softmax classifier. Optimization, Numeric andAnalytic gradients.	4
2	**Neural Networks**	

2.1	Deep feedforward networks/ Multilayer perception: Perceptron, activation functions, Example: Learning XOR, Architecture ofdeep neural network	2
2.2	Back propagation, Gradient-Based Learning.	2
2.3	Convolutional Neural Networks: Convolution, Pooling Layers, spatialarrangement, layer patterns, layer sizing patterns.	3
3	**Training Neural Networks**	
3.1	Initialization, batch normalization, Hyper parameter optimization.	2
3.2	Optimization algorithms: SGD, Momentum, Adagrad, RMS Prop, Adam	2
3.3	Regularization methods: L1 and L2 regularization, Early stopping, drop outs, ensembles, data augmentation, Update rules, transfer learning	2
4	**CNN architectures**	
4.1	AlexNet, VGG Net, ResNet, Inception Net	3
4.2	Object Detection: RCNN, Fast RCNN, Faster RCNN, YOLO, Mask RCNN	3
4.3	Recurrent Neural Networks: RNN, Bidirectional RNN, LSTM, GRU	3
5	**Attention Models, Transformers and Generative Models**	
5.1	Attention: Multimodal attention, Self-Attention	3
5.2	Transformers: BERT and vision transformer	3
5.3	Autoencoders, Variational auto encoders, Generative Adversarial Network	4

Reference Books

1. Ian Goodfellow, YoshuaBengio, and Aaron Courville. Deep learning. MIT press,2016.
2. Francois Chollet. Deep learning with Python. Simon and Schuster, 2021.
3. Ivan Vasilev. Advanced Deep Learning with Python: Design and implement advanced next-generation AI solutions using TensorFlow and PyTorch. Packt Publishing Ltd, 2019.
4. C. M. Bishop, Pattern Recognition and Machine Learning, Springer, 2006
5. Michael A Nielsen. Neural networks and deep learning. Determination press, 2015.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC044	STATIC TIMING ANALYSIS	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble:

1. To understand the concepts of Static Timing Analysis in Industry standarddigital design flow.
2. To study the concept design constraints in ASIC/FPGA designing.
3. To familiarize the various Timing Analysis Concepts and requirements inpractical design flow.

Course Outcomes: The COs shown are only indicative. For each course, there canbe 4 to 6 COs.
After the completion of the course the student will be able to

CO 1	Analyse the STA characteristics of a digital circuit and express the results
CO 2	Evaluate the Standard Cell Library model characteristics
CO 3	Analyse the interconnect parasitics of the circuit and calculate the delay
CO 4	Evaluate the Crosstalk and Noise of circuits based on models.
CO 5	Verify the timing based on the models and calculate the slack

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3							2	
CO 2	3							3	3
CO 3	3		3	3	3			1	1
CO 4	3							1	
CO 5	3							3	3

Assessment Pattern

Bloom's Category	End Semester Examination	
Apply	12 marks/60	20%
Analyse	24 marks/60	40%
Evaluate	38 marks/60	63%
Create	0 marks/60	0

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Micro project/Course based project : 20 marks

Course based task/Seminar/Quiz : 10 marks Test

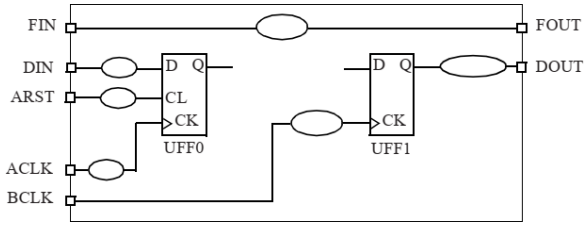
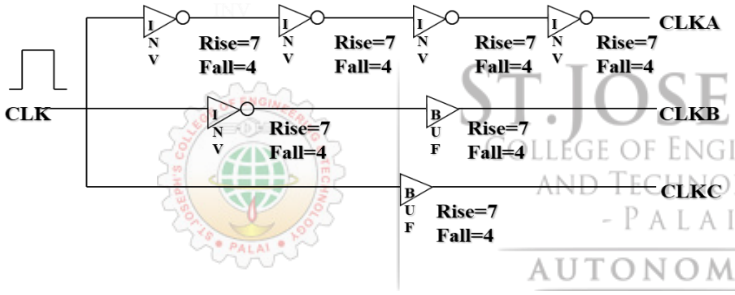
paper, 1 no. : 10 marks

The project shall be done individually. Group projects not permitted. Test papershall include minimum 80% of the syllabus

End Semester Examination Pattern:

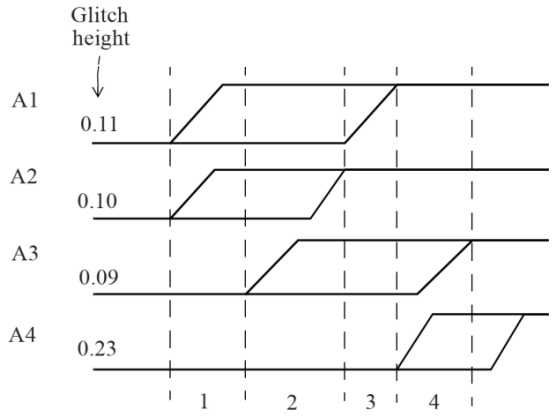
The end semester examination will be conducted by the College. There will be two parts; Part A and Part B. Part A contain 5 numerical questions (such questionsshall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students), with 1 question from each module, having 5 marks for each question. Students shall answer all questions. Part B contains 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each moduleof which student shall answer any five. Each question can carry 7 marks. Total duration of the examination will be 150 minutes

Model Question Paper

		PART A **Answer all questions**	
1		Analyse the STA at Different Design Phases of an ASIC with a neat diagram based on the input?	
2		Evaluate the Interface timing model for a Black Box given in Fig.1.What arethe various timing arcs in the Black Box.  	
		Fig.1	
3.		Analyse the clock circuit for Clock latency with reference Fig 2.  	
		Fig.2	
4.		Apply the State-Dependent Model for XOR gate? Explain the different parameters in the Timing model?	
5.		Evaluate the CMOS cell characteristic and derive the electrically equivalent model specifying the capacitances in the nodes if nets are also considered?	
		Part B **Answer any 5 Questions: 7 marks each – 5 x 7 = 35 marks**	

6.		With respect to the Table given in Fig.3 analyse the various terminologies related to the NLDM(Non Linear Delay model). Based upon the delay tables, calculate the rise delay of the inverter corresponding to an input fall transition of 0.3ns and an output load of 0.16pf. Fig.3	
7.		Evaluate the calculation of Cell Delays using Effective Capacitance method?	
8.		Evaluate the Crosstalk glitch analysis method with a diagram? What are the different types of glitches in Crosstalk glitch analysis?	
9.		Apply the Elmore's delay method for calculation of Interconnect Delays?	
10.		Evaluate the DC and AC thresholds in Crosstalk Glitch calculation?	
11.		Analyse what happens when a cell with one set of slew thresholds drivesother cells with different set of slew threshold settings?	

```
pin (OUT) {
  max_transition : 1.0;
  timing() {
    related_pin : "INP1";
    timing_sense : negative_unate;
    cell_rise(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*  0.16      0.35     1.43 */ \
        /* 0.1 */   "0.0513,  0.1537,  0.5280", \
        /* 0.3 */   "0.1018,  0.2327,  0.6476", \
        /* 0.7 */   "0.1334,  0.2973,  0.7252");
      }
    cell_fall(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*  0.16      0.35      1.43 */ \
        /* 0.1 */   "0.0617,  0.1537,   0.5280", \
        /* 0.3 */   "0.0918,  0.2027,   0.5676", \
        /* 0.7 */   "0.1034,  0.2273,   0.6452");
    }
```

12.		Consider another example where four aggressor nets can cause a rising glitch when the aggressor nets transition. Evaluate the worst possible combination of aggressor switching which results in the largest glitch?  	
		Fig.4	

Syllabus

No	Topic	No. of Lectures
1	**Introduction** Basics; Crosstalk and Noise, Design Flow ; CMOS, FPGA & Asynchronous Designs, STA at Different Phases; Limitations; Power& Reliability Considerations . STA Concepts: CMOS Logic; Modeling of CMOS Cells; Switching Waveform; Propagation Delay; Slew of a Waveform;Skew between Signals; Timing Arcs and Unateness; Min and Max Timing Paths; Clock Domains; Operating Conditions	8
2	**Standard Cell Library** Pin Capacitance; Timing Modeling; Timing Models - Combinational Cells; Timing Models - Sequential Cells; State-Dependent Models; Interface Timing Model for aBlack Box; Advanced Timing Modeling; Power DissipationModeling; Other Attributes in Cell Library; Characterization and Operating Conditions.	8
3	**Interconnect Parasitics:** RLC for Interconnect; Wireload Models; Representation of	8

	Extracted Parasitics; Representing Coupling Capacitances; Hierarchical Methodology; Reducing Parasitics for Critical Nets Delay Calculation: Overview; Cell Delay using Effective Capacitance;Interconnect Delay; Slew Merging; Different Slew Thresholds; Different Voltage Domains; Path Delay Calculation; Slack Calculation.	
4	**Crosstalk and Noise** Overview; Crosstalk Glitch Analysis; Crosstalk Delay Analysis; Timing Verification Using Crosstalk Delay; Computational Complexity; Noise Avoidance Techniques **Configuring the STA Environment**: Specifying Clocks; Generated Clocks; Constraining Input Paths; Constraining Output Paths; Timing Path Groups; Modeling of External Attributes; Design Rule Checks; Virtual Clocks; Refiningthe Timing Analysis; Point-to-Point Specification; Path Segmentation	8
5	**Timing Verification:** Setup Timing Check; Hold Timing Check; Multicycle Paths; False Paths; Half-Cycle Paths; Removal Timing Check; Recovery Timing Check; Timing across Clock Domains; Examples; Multiple Clocks **Interface Analysis**: IO Interfaces; SRAM Interface **Robust Verification**: On-Chip Variations; Time Borrowing; Data to Data Checks; Non-Sequential Checks; Clock Gating Checks; Power Management; Backannotation; Sign-off Methodology	8

Reference Books

1. J.Bhasker, Rakesh Chadha, "Static Timing Analysis for Nanometer Designs, A practical approach", Springer publications.
2. Gangadharan, Sridhar, Churiwala, Sanjay "Constraining Designs for Synthesis and Timing Analysis": A Practical Guide to Synopsys Design Constraints (SDC), Springer publications.
3. Churiwala, Sanjay, Garg, Sapan "Principles of VLSI RTL Design" A Practical Guide, Springer publications.
4. Maheshwari, Naresh, Sapatnekar, S. "Timing Analysis and Optimization of Sequential Circuits" Springer publications.
5. HimanshuBhatnagar "Advanced ASIC Chip Synthesis" Using Synopsys Design Compiler Physical Compiler and PrimeTime, Springer publications.

Syllabus and Course Plan

(For 3 credit courses, the content can be for 40 hrs and).

No	Topic	No. of Lectures
1	**Introduction**	
1.1	Basics; Crosstalk and Noise, Design Flow ; CMOS, FPGA & Asynchronous Designs, STA at Different Phases; Limitations; Power& Reliability Considerations .	**4**
1.2	STA Concepts: CMOS Logic; Modeling of CMOS Cells; Switching Waveform; Propagation Delay; Slew of a Waveform;Skew between Signals; Timing Arcs and Unateness; Min and Max Timing Paths; Clock Domains; Operating Conditions	**4**
2	**Standard Cell Library**	
2.1	Pin Capacitance; Timing Modeling; Timing Models - Combinational Cells; Timing Models - Sequential Cells;	**4**
2.2	State-Dependent Models; Interface Timing Model for a Black Box; Advanced Timing Modeling; Power Dissipation Modeling; Other Attributes in Cell Library; Characterization and Operating Conditions.	**4**
3	**Interconnect Parasitics:**	
3.1	RLC for Interconnect; Wireload Models; Representation of Extracted Parasitics; Representing Coupling Capacitances; Hierarchical Methodology; Reducing Parasitics for Critical Nets	**4**
3.2	Delay Calculation: Overview; Cell Delay using Effective Capacitance; Interconnect Delay; Slew Merging; Different Slew Thresholds; Different Voltage Domains; Path Delay Calculation; Slack Calculation.	**4**
4	**Crosstalk and Noise**	
4.1	Overview; Crosstalk Glitch Analysis; Crosstalk Delay Analysis; Timing Verification Using Crosstalk Delay; Computational Complexity; Noise Avoidance Techniques	**4**
4.2	**Configuring the STA Environment**: Specifying Clocks; Generated Clocks; Constraining Input Paths; Constraining Output Paths; Timing Path Groups; Modeling of External Attributes; Design Rule Checks; Virtual Clocks; Refining the Timing Analysis; Point-to-Point Specification; Path Segmentation	**4**
5	**Timing Verification:**	

5.1	Setup Timing Check; Hold Timing Check; Multicycle Paths; False Paths; Half-Cycle Paths; Removal Timing Check; Recovery Timing Check; Timing across Clock Domains; Examples; Multiple Clocks	**2**
5.2	**Interface Analysis**: IO Interfaces; SRAM Interface	**2**
5.3	**Robust Verification**: On-Chip Variations; Time Borrowing; Data to Data Checks; Non-Sequential Checks; Clock Gating Checks; Power Management; Backannotation; Sign-off Methodology	**2**

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC045	SIGNAL COMPRESSION	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble: This course aims to impart the knowledge on information theory anddifferent compression techniques on data, image, audio and video in depth.

Prerequisite:

1. Basic knowledge in Information theory
2. Basic knowledge in digital signal processing
3. Basic knowledge in Frequency transform

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply different coding algorithms for data, audio, image and Video compression.
CO 2	To Implement basic compression algorithms with MATLAB and its equivalent open-source environments
CO 3	Design and implement some basic compression standards
CO 4	Critically analyse different approaches of compression algorithms in multimedia related mini projects
CO 5	Apply the theory and practice of video compression methods as well as its applications in digital media and communication systems in everyday use.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3								
CO 2	3	2		2				3	3
CO 3	3		3	3	3				
CO 4	3	2							
CO 5	3							3	3
CO 6	3		3	3				3	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	50
Analyse	40
Evaluate	10
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer-reviewed original publications (minimum10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15 marksTest paper, 1 No.: 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7 marks.

Model Question Paper

QP CODE: **PAGES: 2**

Reg No: **Name:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code:

Course Name: Signal Compression

Max. Marks: 60 **Duration: 2.5 Hours**

PART A

Answer all Questions. Each question carries 5 Marks

1. Explain Huffman Coding algorithm?
2. Derive a relation which indicates the change in SNR of a uniform quantizer,for a uniformly distributed source, for a bit change?
3. Explain the steps in transform coding?
4. Explain how spectral and temporal masking helps in speech compression?
5. Explain the conversion of CCIR 601 frame to MPEG-SIF frame?

(5x5=25 Marks)

PART B

Answer 5 questions, one from each module. Each question carries 7 marks

6. Encode the sequence 'THISISTHE' using LZW algorithm.

7. Find the number of bits needed by an EZW coder, after three iterations, forthe decomposition given below:

26	6	13	10
-7	7	6	4
4	-4	4	-3
2	-2	-2	0

8. Explain JPEG encoder used for lossy image compression?
9. a)Explain the sub band coding algorithm with necessary block diagrams?
   b) Is mp3 standard backward compatible? Justify your answer.

10. Explain how Dolby AC3 (Dolby Digital) standard is used for audio compression?
11. Explain Federal standard 1016 speech coder?
12. Explain how quantization and coding is done and rate control is achieved in H.261 standard?

(5x7=35 Marks)

Syllabus

Module 1: Need for compression – Taxonomy of compression Algorithms - Elementsof Information Theory – Error Free Compression – Lossy Compression, Huffman Coding, its variants, Optimality, Arithmetic Coding and its variants, Run Length Coding, Dictionary Techniques , Lempel-Ziv coding, Predictive Coding, Burrows Wheeler Transform, Dynamic Markov Compression. Golomb codes, Rice codes, Tunstall codes

Module 2: Quantization, Uniform & Non-uniform, optimal and adaptive quantization, vector quantization, structures for VQ, Optimality conditions for VQ, Predictive Coding , Differential Encoding

Module 3: Image compression: Predictive techniques, DM, PCM, DPCM: Optimal Predictors and Optimal Quantization, Contour based compression, Transform Coding, JPEG Standard, Sub-band coding algorithms: Design of Filter banks, Wavelet based compression, EZW, SPIHT, JPEG 2000 standards, JBIG, JBIG2,JPEG-LS, CALIC.

Module 4 Audio compression techniques, Standards for audio compression in multimedia applications, MPEG audio encoding and decoding, Dolby AC-3 standard.
Speech compression techniques, Vocoders, Speech compression - quality measures, waveform coding, source coders, Speech compression standards for personal communication systems

Module 5: Video compression techniques and standards, Motion estimation and compensation techniques, H.261, Dolby Digital 5.1.

Course Plan (40 hrs)

No	Topic	No. of Lectures
1	**MODULE –I**	**(8 hrs.)**
1.1	Need for compression – Taxonomy of compression Algorithms -	1
1.2	Elements of Information Theory – Lossy and lossless Compression, Distortion criteria, Differential Entropy, Rate Distortion Theory,	2

1.3	Huffman Coding, its variants, Optimality, Arithmetic Coding and its variants, Run Length Coding,	2
1.4	Dictionary Techniques , Lempel-Ziv coding	1
1.5	Predictive Coding, Burrows Wheeler Transform, Dynamic Markov Compression.	2
2	**MODULE –II**	**(6 hrs.)**
2.1	Quantization, Uniform & Non-uniform,	1
2.2	optimal and adaptive quantization, vector quantization, structures for VQ,	2
2.3	Optimality conditions for VQ, Predictive Coding , Differential Encoding.	2
2.4	LBG algorithm, Tree structured VQ	2
3	**MODULE III**	**(8 hrs.)**
3.1	Image compression: Predictive techniques, DM, PCM, DPCM:	2
3.2	Transform Coding: Transforms–KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients	2
3.3	Application to Image compression– Sub-band coding algorithms: Design of Filter banks, Wavelet based compression,	2
3.4	JPEG Standards: ,JPEG,JPEG 2000 standards, JBIG, JBIG2, JPEG-LS, EZW, SPIHT, CALIC.	2
4	**MODULE IV**	**(12 hrs.)**
4.1	Audio compression techniques, Standards for audio compression in multimedia applications,	3
4.2	MPEG audio encoding and decoding, Dolby AC-3 standard.	3
4.3	Speech compression techniques, Vocoders, Speech compression - quality measures	3
4.4	waveform coding, source coders, Speech compression standards for personal communication systems	3
5	**MODULE V**	**(6 hrs.)**
5.1	Video compression techniques and standards,	2
5.2	Motion estimation and compensation techniques,	2
5.3	H.261, Dolby Digital 5.1.	2

Reference Books

1. Khalid Sayood, Introduction to Data Compression, Morgan Kaufmann Publishers., Second Edn. 2005.
2. David Salomon, Data Compression: The Complete Reference, Springer Publications, 4th Edn. 2006
3. N.Jayant and P.Noll, "Digital Coding of Waveforms: Principles and Applications to Speech and Video", Prentice Hall, USA,1984
4. K.R.Rao, P.C.Yip, The Transform and Data Compression Handbook, CRC Press. 2001
5. R.G.Gallager, Information Theory and Reliable Communication, John Wiley& Sons, Inc., 1968
6. Ali N. Akansu, Richard A. Haddad, Multiresolution Signal Decomposition: Transforms, Subbands and Wavelets, Academic Press., 1992
7. Martin Vetterli, Jelena Kovacevic, Wavelets and Subband Coding, Prentice Hall Inc., 1995.
8. . Z. Li and M.S. Drew, Fundamentals of Multimedia, Pearson Education (Asia) Pte. Ltd., 2004.

SEMESTER II

INTERDISCIPLINARY ELECTIVE

INTERDISCIPLINARY ELECTIVE						
SLOT	**SL NO**	**COURSE CODE**	**COURSE NAME**	**L-T-P**	**HOURS**	**CREDIT**
E	1	24SJ2EEC083	AUTOMOTIVE ELECTRONICS	3-0-0	3	3
	2	24SJ2EEC084	MEMS AND SENSORS	3-0-0	3	3
	3	24SJ2EEC085	NANO MATERIALS FOR DRUG DELIVERY	3-0-0	3	3

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EE C083	AUTOMOTIVE ELECTRONICS	INTER-DISCIPLINARY ELECTIVE	3	0	0	3

Preamble: The purpose of this course is to provide an awareness of Automotive Electronics. As an outcome of the course the students will be aware of the technical details of Electronics Engineering in Automotive industry, the current trends and challenges.

Course Outcomes: After the completion of the course the student will be able to:

CO#	CO
CO1	Understand the fundamentals of vehicle electronic systems and integration of electronic components in vehicle system architecture.
CO2	Understand the various communication technologies on board vehicles
CO3	Understand the working of various control algorithms implemented in vehicles for the purpose of automation
CO4	Apply the knowledge of electronics for safety and security in vehicle automation
CO5	Understand the emerging trends in automotive electronics

Program Outcomes:

PO#	PO
PO1	An ability to independently carryout research/investigation and development work in engineering and allied streams
PO2	An ability to communicate effectively,write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with Society at large.
PO3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program.The mastery should be at a level higher than the requirements in the Appropriate bachelor's program
PO4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.

PO6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3								
CO 2	3							3	3
CO 3	3		3	3	3				
CO 4	3								
CO 5	3							3	3
CO 6	3		3	3				3	3

Assessment Pattern

Bloom's Category		**Continuous Assessment Tests**	**End Semester Examination**
		Test [%] (10 marks)	**Institute Exam[%] (60 marks)**
Remember	K1	20	20
Understand	K2	60	60
Apply	K3	20	20
Analyse	K4		
Evaluate			
Create			

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern (Elective):

Preparing a review article based on peer-reviewed original publications(minimum10 publications shall be referred): 15 marks
Course-based task/Seminar/Data collection and interpretation: 15marks
(Group projects not permitted)
Test paper, 1 No. : 10 marks
Test paper shall include a minimum of 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts: Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions, with a minimum of one question from each module of which students should answer any five. Each question can carry 7marks.

Model Question Paper

PAGES: 1 **Slot**

Name: **Reg No:**

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: 24SJ2EEC083

Course Name: A u t o m o t i v e E l e c t r o n i c s

Max.Marks: 60 **Duration: 2.5Hours**

PART A

Answer all Questions. Each question carries 5 marks

1. a) State the functions of Motronic engine-management.
   b) Explain the working principle of fuel injector.
2. Illustrate basic CAN module with block diagram and explain.
3. Explain the principle of on board diagnostics in automotive electronics.
4. Illustrate the concept of anti slip regulation in automotive safety systems.
5. Explain the concept of V2V communication.

(5x5=25Marks)

PART B

Answer any 5 questions. Each question carries 7 marks

6. Illustrate Electronic ignition system configuration with suitable diagram.
7. Justify the need for a communication network in a vehicle.
8. a) Differentiate between Cruise control and Traction Control. (4)
   b) Explain the concept of Actuator Limiting. (3)
9. Illustrate the principle of interfacing an A/D converter with a temperature sensor. State the specifications of the modules used.
10. a) Explain blind spot detection in vehicles. (4)
    b) Identify the pedestrian safety measures available in modern cars (3)
11. Illustrate the autonomous driving system architecture with block diagram.
12. Explain the working of hybrid vehicles with a block diagram,.

Syllabus

Module 1: Introduction to Automotive Electronics (7Hrs)

Overview of vehicle electronic systems,Integration of electronic components and systems in vehicles, Vehicle System Architecture – Sensors – Actuators – Embedded processors and micro-controllers, Introduction to Electronic Instrumentation for sensors: temperature, distance, velocity, speedometer, anti-collision. limitations, topologies and processing for sensors, DA/AD converters, Interfacing ADC/DAC to peripherals and sensors

Module 2: Automotive Communications Systems (7Hrs)

Introduction to communications standards, Introduction to networks, safety critical issues and reliability, Communication protocols for automotive applications, CAN- protocol layers, contentbased addressing, Hardware- basic CAN module, Basic block level working principle of LIN, MOST, Bluetooth & FlexRay, Telematics for automotive applications, GPRS, GPS in automotiveenvironment

Module 3: Automotive Control and Power Systems (7Hrs)

ECU – Electronic Engine Control, Electronic control methods (analog and digital), Stability algorithms for control-cruise control, traction control, Actuator limiting, wind-up and gain scheduling.Energy management strategies: regenerative braking, start-stop, torque boost, Sensing and control systems, Automotive Diagnostics- OBD – Onboard Diagnostics

Module 4: Automotive Safety Systems and ADAS (7Hrs)

Introduction to safety systems, Passive system electronics: Airbag and sensors, Active systems electronics: Anti lock braking system (ABS), Electronic Stability Program (ESP), Anti-slip regulation (ASR), Driver Assistance Systems**:** Advanced active systems electronics: ACC , Active safety system applications: lane detection, blind spot, crash avoidance control electronics, Basics of ADAS, Power Steering, Automatic climate control

Module 5: Advancements in automotive electronics (7Hrs)

Introduction to Autonomous driving-system architecture overview, Navigation systems –VANET, vision intelligence, computational intelligence, smart traffic systems, security, EV- classification, benefits and challenges, Basic concepts and challenges of Hybrid vehicles, fuel cell powered vehicles.

Text Books:

1. William B.Ribbens, "Understanding Automotive Electronics", 6thEdition, Elsevier Publishing.
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, Springer Vieweg, John Wiley Sons.

References:

1. Hybrid & Electric Vehicles -A CRC Press FREEBOOK
2. Creating Autonomous Vehicle Systems -SYNTHESIS LECTURES ON COMPUTER SCIENCE MORGAN & CLAYPOOL PUBLISHERS
3. A Progressive Review: Emerging Technologies for ADAS Driven Solutions- Jaswanth Nidamanuri , Chinmayi Nibhanupudi, Rolf Assfalg, and Hrishikesh Venkataraman, IEEE TRANSACTIONS ON INTELLIGENT VEHICLES, VOL. 7, NO. 2, JUNE 2022
4. Hillier's Fundamentals of Motor Vehicle Technology5th Edition Book 3,V.A.W. Hillier & David R. Rogers

Course Plan

	Topic	No.of Lectures
	Module 1: Introduction to Automotive Electronics (7Hrs)	
1.1	Overview of vehicle electronic systems	1
1.2	Integration of electronic components and systems in vehicles - Description of VSA- Sensors – Actuators- Embedded processors and micro controllers	1
1.3	Sensors in detail: temperature, distance, velocity, speedometer, anti-collision, limitations, topologies and processing for sensors	2
1.4	DA/AD converters,	1
1.5	Interfacing ADC to peripherals and to sensors	1
1.6	Interfacing DAC to peripherals and to sensors	1
	Module 2: Automotive Communications Systems (7Hrs)	
2.1	Introduction to communications standards , networks, safety critical issues and reliability	1
2.2	Communication protocols for automotive applicationCAN	2
2.3	Basic block level working principle of LIN, MOST, Bluetooth, & FlexRay	2
2.4	Telematics for automotive applications	1
2.5	GPRS, GPS for use in and automotive environment	1
	Module 3: Automotive Control and Power Systems (7Hrs)	
3.1	ECU, Electronic control methods (analog and digital)	1
3.2	Stability algorithms for control (cruise control, traction control)	2
3.3	Actuator limiting, wind-up, gain scheduling	1
3.4	Energy management strategies: regenerative braking, start-stop, torque boost, Sensing and control systems	2
3.5	Automotive diagnostics-OBD	1
	Module 4: Automotive Safety Systems and ADAS (7Hrs)	
4.1	Introduction to safety systems: Passive and Active systems electronics.	1
4.2	Antilock-braking system (ABS), Electronic Stability Program (ESP), Anti-slip regulation (ASR)	1
4.3	Driver Assistance Systems: Advanced active systems electronics: ACC, Basics of ADAS	2
4.4	Active safety system applications: lane detection, blind spot, crash avoidance control electronics	2
4.5	Power Steering , Automatic climate control	1

	Module 5: Advancements in automotive electronics (7Hrs)	
5.1	Introduction to Autonomous driving-system architecture-overview	1
5.2	Navigation systems, VANET,.vision intelligence, computational intelligence	2
5.3	Smart traffic systems, security	**1**
5.4	Basics of EV- classification, benefits, challenges	**1**
5.5	Basic concepts and challenges of Hybrid vehicles, fuel cell powered vehicles	**2**

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC084	MEMS AND SENSORS	INTERDISCIPLINARY ELECTIVE	3	0	0	3

Course Objectives

- Introduces students to the need of rapidly emerging, area of MEMSandmicrosystem in engineeringand its applications in sensor technology
- Enable the students to understand the various sensing and actuationmechanisms.

Prerequisite: nil

Course Outcomes: After the completion of the course the student will be able to

CO1	Identify structural and sacrificial materials for MEMS
CO2	Describe the fabrication steps in designing of various MEMS devices.
CO3	Apply principles for the design of Sensor and actuators
CO4	Apply MEMS for different applications in various fields of engineering

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3								
CO 2	3							3	3
CO 3	3		3	3	3				
CO 4	3								
CO 5	3							3	3
CO 6	3		3	3				3	3

Assessment Pattern

Bloom'sCategory	Continuous Assessment Tests		End Semester Examination [%] (60Marks)
		Test1 [%] (10Marks)	
Remember		10	20
Understand		20	40
Apply		10	20
Analyse		10	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE (Marks)	ESE (Marks)	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation: 40 marks Preparing a review article based on peer reviewed Original publications (minimum 10 publications shall be referred) : 15 marks Course based task/Seminar/Micro project : 15 marksTest paper 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination: 60 marks The end semester examination will be conducted by the respective college. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one questionfrom each module of which student should answer any five. Each question can carry 7 marks.

	SYLLABUS
1	**MODULE I**
Introduction: Introduction to MEMS and Microsystems, MEMS Classification, MEMS versus Microelectronics, Applications of MEMS in Various Industries, Some Examplesof Microsensors, Microactuators, and Microsystems, Materials for MEMS, Laws of Scaling in miniaturization	
2	**MODULE II**
MEMS Fabrication: Structure of Silicon, Single Crystal Growth Techniques, Photolithography, Oxidation, Diffusion, Ion Implantation, Physical Vapor Deposition, Chemical Vapor Deposition, Bulk Micromachining: Overview of Etching, Isotropic and Anisotropic Etching, Wet Etchants, Etch Stop Techniques, Dry Etching, Surface Micromachining, LIGA, SLIGA, Wafer Bonding, Electroplating	
3	**MODULE III**
Microsensors and Microactuators: Basic Modeling Elements in Mechanical, Electrical and Thermal Systems, Types of Beams: Cantilevers, Bridges, Fixed- Guided beams, Electrostatic sensing and Actuation: Parallel plate capacitor, Applications of parallel plate capacitors: Inertial sensor, Pressure sensor, Flow sensor, Parallel plate Actuators, Piezoresistive Sensors: Origin and Expressions of Piezoresistivity, Piezoresistive Sensor Materials, Applications of Piezoresistive Sensors, Piezoelectric Sensing and Actuation, Thermal Sensing and Actuation:Sensors and Actuators based on Thermal Expansion, Thermocouples, Thermoresistors, Shape Memory Alloy, Applications: Inertial sensors, Flow sensors, Infrared sensors	
4	**MODULE IV**

Layout, Simulation Tools, Packaging and Characterization techniques: Introduction of layout, Simulation Tools, General considerations in Packaging , Bonding techniques for MEMS and Various Characterization Techniques for MEMS Devices	
5	**MODULE V**
Advances in MEMS:RF-MEMS: MEMS devices for RF Applications: RF MEMS Switches and their applications, High-Q Capacitors and Inductors and Their	

Applications in RF Circuits, Overview of Optical MEMS , Chemical-Bio MEMS and Nanoelectromechanical Systems

Text books

- MEMS and Microsystems design and manufacture by Tai-Ran Hsu, Tata McGraw Hill.
- MEMS by N. P. Mahalik, Tata McGraw Hill.
- Foundations of MEMS by Chang Liu, Pearson Prentice Hall.

Reference books

- Sensors and Transducers by M. J. Usher, McMillian Hampshire.
- Analysis and Design Principles of MEMS Devices by Minhang Bao, Elsevier.
- Fundamentals of Microfabrication by M. Madou, CRC Press.
- Microsensors by R.S. Muller, Howe, Senturia and Smith, IEEE Press.
- Semiconductor Sensors by S. M. Sze, Willy Inderscience Publications.

COURSE CONTENTS AND LECTURE SCHEDULE

No.		No. of Hours
	MODULE 1	
1.1	Introduction to MEMS and Microsystems, MEMS Classification, MEMS versus Microelectronics,	1
1.2	Applications of MEMS in Various Industries, Some Examples of Microsensors, Microactuators, and Microsystems	1
1.3	Materials for MEMS,	2
1.4	Laws of Scaling in miniaturization	1
	MODULE II	
2.1	Structure of Silicon, Single Crystal Growth Techniques,	1
2.2	Photolithography, Oxidation,	1
2.3	Diffusion, Ion Implantation,	1
2.4	Physical Vapor Deposition, Chemical Vapor Deposition,	1
2.5	Bulk Micromachining: Overview of Etching, Isotropic and Anisotropic Etching,	1
2.6	Wet Etchants, Etch Stop Techniques, Dry Etching	1

2.7	Surface Micromachining	1
2.8	LIGA, SLIGA	2
2.9	Wafer Bonding, Electroplating	1
	MODULE III	
3.1	Microsensors and Microactuators: Basic Modeling Elements in Mechanical, Electrical and Thermal Systems,	1
3.2	Types of Beams: Fixed-Free (Cantilevers), Fixed-Fixed (Bridges), Fixed-Guided beams,	1
3.3	Electrostatic sensing and Actuation: Parallel plate capacitor,	1
3.4	Applications of parallel plate capacitors: Inertial sensor,	1
3.5	Pressure sensor, Flow sensor, Parallel plate Actuators,	1
3.6	Piezoresistive Sensors: Origin and Expressions of Piezoresistivity, Piezoresistive Sensor Materials,	1
3.7	Applications of Piezoresistive Sensors,	1
3.8	Piezoelectric Sensing and Actuation,	1
3.9	Thermal Sensing and Actuation: Sensors and Actuators based on Thermal Expansion,	1
3.10	Thermocouples, Thermoresistors,	1
3.11	Shape Memory Alloy, Applications: Inertial sensors, Flow sensors, Infrared sensors	2
	MODULE IV	
4.1	Introduction of layout, Simulation Tools,	1
4.2	General considerations in Packaging and bonding techniques in MEMS	2
4.3	Various Characterization Techniques for MEMS Devices	1
	MODULE V	
5.1	Advances in MEMS: RF-MEMS: MEMS devices for RF Applications:	1
5.2	RF MEMS Switches and their applications,	1

5.3	High-Q Capacitors and Inductors and Their Applications in RF Circuits,	1
5.4	Overview of Optical MEMS ,	1
5.5	Chemical-Bio MEMS and Nanoelectromechanical Systems	1

Model Question Paper

ST. JOSEPH'S COLLEGE OF ENGINEERING AND TECHNOLOGY, PALAI (AUTONOMOUS)

Second Semester M.Tech Degree Examination

Course: 24SJ2EEC084MEMS and Sensors Time: 150 Minutes Max. Marks: 60

PART A

Answer All Questions

1	Mention the criteria for selecting materials for the masks used in etching. List four materials used as masks.	5
2	Define etch stop? List different methods used to stop etching and explain one with sketches	5
3	Explain with neat sketches the type of mechanical beams and boundary conditions associated with supports	5
4	State the various levels of micro system packaging	5
5	With neat sketches explain the construction and working of a shunt type RF MEMS switch.	5

PART B

Answer any five question

6	A silicon substrate is doped with phosphorus ions at 100 KeV. Assume the maximum concentration after the doping is 30 x $10^{18}/cm^3$. Find: (a) the dose, Q, (b) the dopant concentration at the depth 0.15 µm, (c) the depth at which the dopant concentration is at 0.15% of the maximum value. (Given: Rp = 135 nm and ΔRp = 53.5 x 10^{-7}cm at 100 KeV energy level).	*7*
7	Explain in the light of scaling, assuming a 10 times reduction of size of the actuator. Which of the electrostatic and electromagnetic forces are best suited for micro device actuation and why?	*7*
8	Explain the purpose of micro cantilevers in MEMS systems. What is the relevance of Spring constant (k) of the mechanical structure in the microsystems.	*7*

9	Explain the principle of operation of the following micro sensors (i) Comb drives (ii) Shape Memory Alloys	7
10	Explain the challenges involved in BioMEMS. List three applications of BioMEMS.	7
11	Explain Various bonding techniques associated with MEMS and their implications on packaging	7
12	Explain the LIGA process associated with MEMS fabrication with suitable sketches	7

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
24SJ2EEC085	NANO MATERIALSFOR DRUG DELIVERY	INTERDISCIPLINARYELECTIVE	3	0	0	3

Preamble: To inspire the students with interest to investigate role of newnanomaterials and devices drug delivery.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Familiarize the concepts of nano materials for drug delivery
CO 2	Investigate the use of nano materials for drug delivery
CO 3	Investigate the use of nanodevices for drug targeting

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PSO1	PSO2
CO 1	3		1		1			1	
CO 2	3					2	2	3	3
CO 3	3		3	3	3		1		

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	40
Evaluate	
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern

Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks Test paper, 1 no. : 10 marks
The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A will contain 5 short answerquestions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Syllabus and course plan

No	Topic	No. of Lectures
1	**Nanomedicines**	
1.1	Basic concepts in the design, specification and desired features of nanomedicine and general process steps involved in their preparation Nanomedicines for various disease conditions: infectious diseases, neurological diseases, pulmonary disorders, cardiovascular diseases	4
1.2	cancer: nano-chemotherapy, - radiation therapy, - immunotherapy, - nuclear medicine therapy, -photodynamic therapy, - photothermal and RF hyperthermia therapy, scintillation therapy, gene-therapy DNA, RNA delivery. Theranostic nanomedicines: Basic concept, multifunctional nanomedicines for theranosis	4
2	**Drug Delivery Systems**	
2.1	Administration Routes: Oral Drug Delivery, Features of Gastrointestinal tract (GI), Targeting of drugs in the GI tract.	4
2.2	Design and fabrication of oral systems - Dissolution controlled, diffusion controlled, osmotic controlled, chemically controlled release, Intravenous Drug Delivery - Factors controlling pharmacokinetics of IV formulations, Concept of opsonization	4
3	**Drug Delivery Devices**	
3.1	Transdermal Drug Delivery, Structure of human skin and theoretical advantages of the transdermal route, Transdermal penetration of drugs, adhesion, bioactivity.	4
3.2	Intranasal Drug Delivery - Nasal physiology and intranasal Drug Administration, Nasal drug delivery devices, Ocular Drug Delivery devices; Miscellaneous Drug Delivery	4
4	**Advanced Drug Delivery**	
4.1	Concept of Drug Targeting; Prodrug and Bioconjugation; Nanoscale Drug Delivery Systems - Advantages of nanodrug delivery – Improvements in pharmacokinetics, bioavailability, biodistribution; Concepts of controlled and sustained drug delivery, How nanoparticles pass barriers; Surface modification of nanoparticulate carriers	4

4.2	Nanocarriers for drug delivery - Lipid based pharmaceutical nanoparticles – Liposomes, Solid Lipid Nanoparticles, Nanostructured Lipid Carriers, Cubosomes and Hexosomes, Polymeric Micelles, DNA- Based Nanomaterials, Dendrimers, Polymeric nanoparticles, Inorganic nanoparticles, Hydrogels for controlled drug delivery	4
5	**Active and passive nanocarriers**	
5.1	Concept of targeting, Site Specific Drug delivery utilizing Monoclonal Antibodies, Peptides, Other Biomolecules, Stimuli-Responsive Target Strategies; Implants; Protein and Peptide Drug Delivery; Delivery of Nucleic Acids	3
5.2	Delivery of Vaccines; Aptamers in Advanced Drug Delivery; Biomimetic Self-Assembling Nanoparticles	2
5.3	Nanotechnology Challenges; Regulatory Considerations and Clinical Issues in Advanced Drug Delivery	3

Books-

1. Drug Delivery Systems, Pieter Stroeve and MortezaMahmoudi, World Scientific Series: From
2. Biomaterials towards Medical Devices, Vol I, 2018.
3. Nanoparticulates as Drug Carriers, Vladimir Torchillin, Imperial College Press, 2006
4. Drug Delivery Systems, Third Edition, Vasant V Ranade, John B. Cannon, by CRC Press, 2011

Department of

Electronics and Communication Engineering

Vision

Develop into a center of excellence in Electronics and Communication Engineering contributing to socio-economic progress.

Mission

- To develop and maintain adequate infrastructure for a pace-setting Electronics and Communication engineering.
- To bring up a team of committed, proficient and research-oriented electronics and communication engineering faculty.
- To nurture students into ethical, emotionally strong and technically competent graduates to meet the dynamic challenges of the society.