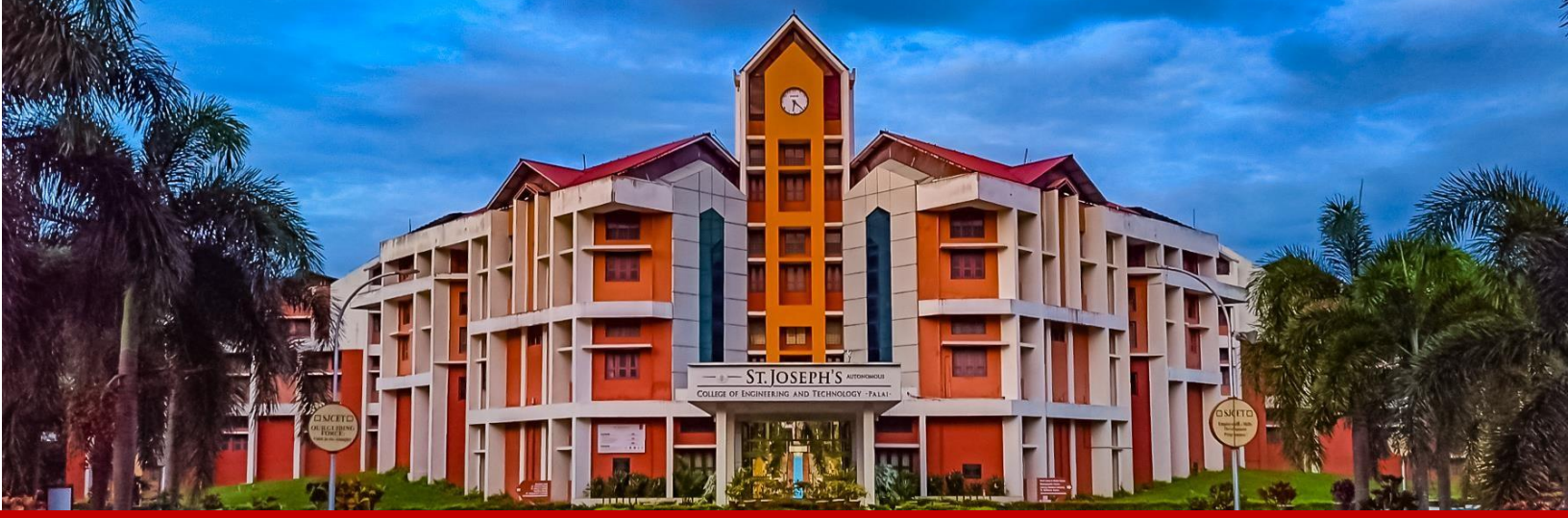
ST. JOSEPH'S
COLLEGE OF ENGINEERING
AND TECHNOLOGY,
- PALAI -
AUTONOMOUS

Choondacherry P.O., Pala, Kottayam - 686579
Kerala, India



SYLLABUS

B. Tech.

ELECTRONICS AND COMMUNICATION ENGINEERING

2024 SCHEME

www.sjcetpalai.ac.in

Signed By:Devassia V P
Reason: Approved by SJCET Academic Council held on 13.05.2025

COURSES

SEMESTER – III

SEMESTER – IV

ST. JOSEPH'S
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Syllabus- Third Semester

THIRD SEMESTER (July-December)														
Sl. No:	**Slot**	**Course Code**	**Course Type**	**Course Category**	**Course Title (Course Name)**	**Credit Structure**				**SS**	**Total Marks**		**Credits**	**Hrs./ Week**
						L	**T**	**P**	**R**		**CIE**	**ESE**		
1	A	**24SJGYMAT301**	BSC	GC	Mathematics for Electrical Science and Physical Science-3	3	0	0	0	4.5	40	60	3	3
2	B	**24SJPCECT302**	PC	PC	Solid State Devices	3	1	0	0	5	40	60	4	4
3	C	**24SJPCECT303**	PC	PC	Analog Circuits	3	1	0	0	5	40	60	4	4
4	D	**24SJPBECT304**	PC-PBL	PB	Logic Circuit Design	3	0	0	1	5.5	60	40	4	4
5	F	**24SJGYEST305**	ESC	GC	Introduction to Artificial Intelligence and Data Science	3	1	0		5	40	60	4	4
6	G S3/S4	**24SJICHUT346**	HMC	IC	Economics for Engineers	2	0	0	0	3	50	50	2	2
		24SJICHUT347			Engineering Ethics and Sustainable Development									
7	L	**24SJPCECL307**	PCL	PC	Analog Circuits Lab	0	0	3	0	1.5	50	50	2	3
8	Q	**24SJPCECL308**	PCL	PC	Logic Circuit Design Lab	0	0	3	0	1.5	50	50	2	3
9	R/M		VAC		Remedial/Minor Course	3	1	0	0	5			4*	4*
Total										**31/ 36**			**25/29***	**27/31***
Bridge Course for Lateral Entry Students: Total 15 Hrs.														

**No Grade Points will be awarded for the MOOC course and I slot course.*

SEMESTER S3

MATHEMATICS FOR ELECTRICAL SCIENCE AND PHYSICAL SCIENCE – 3 (24SJGYMAT301)

Course Code	24SJGYMAT301	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Basic knowledge in complex numbers.	Course Type	Theory

Course Objectives:

1. To introduce the concept and applications of Fourier transforms in various engineering fields.
2. To introduce the basic theory of functions of a complex variable, including residue integration and conformal transformation, and their applications

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Fourier Integral, From Fourier series to Fourier Integral, Fourier Cosine and Sine integrals, Fourier Cosine and Sine Transforms, Linearity, Transforms of Derivatives, Fourier Transform and its inverse, Linearity, Transforms of Derivative. **(Text 1: Relevant topics from sections 11.7, 11.8, 11.9)**	9
2	Complex Function, Limit, Continuity, Derivative, Analytic functions, Cauchy-Riemann Equations (without proof), Laplace's Equations, Harmonic functions, Finding harmonic conjugate, Conformal mapping, Mappings of w= z^2 , $w=e^z$, $w = \frac{1}{z}$, $w= sinz$. **(Text 1: Relevant topics from sections 13.3, 13.4, 17.1, 17.2, 17.4)**	9

3	Complex Integration: Line integrals in the complex plane (Definition & Basic properties), First evaluation method, Second evaluation method, Cauchy's integral theorem (without proof) on simply connected domain,	9
	Independence of path, Cauchy integral theorem on multiply connected domain (without proof), Cauchy Integral formula (without proof). **(Text 1: Relevant topics from sections 14.1, 14.2, 14.3)**	
4	Taylor series and Maclaurin series, Laurent series (without proof), Singularities and Zeros – Isolated Singularity, Poles, Essential Singularities, Removable singularities, Zeros of Analytic functions – Poles and Zeros, Formulas for Residues, Residue theorem (without proof), Residue Integration- Integral of Rational Functions of cosθ and sinθ. **(Text 1: Relevant topics from sections 15.4, 16.1, 16.2, 16.3, 16.4)**	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
2 Questions from each module. Total of 8 Questions, each carrying 3 marks (8x3 =24marks)	Each question carries 9 marks. Two questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. (4x9 = 36 marks)	60

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Determine the Fourier transforms of functions and apply them to solve problems arising in engineering.	K3
CO2	Understand the analyticity of complex functions and apply it in conformal mapping.	K3
CO3	Apply Cauchy's integral theorem and Cauchy's integral formula to compute complex integrals .	K3
CO4	Understand the series expansion of complex function about a singularity and apply residue theorem to compute real integrals.	K3

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	-	2	-	-	-	-	-	-	2
CO2	3	3	-	2	-	-	-	-	-	-	2
CO3	3	3	-	2	-	-	-	-	-	-	2
CO4	3	3	-	2	-	-	-	-	-	-	2

Text Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Advanced Engineering Mathematics	Erwin Kreyszig	John Wiley & Sons	10th edition, 2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Complex Analysis	Dennis G. Zill, Patrick D. Shanahan	Jones & Bartlett	3rd edition, 2015
2	Higher Engineering Mathematics	B. V. Ramana	McGraw-Hill Education	39th edition, 2023
3	Higher Engineering Mathematics	B.S. Grewal	Khanna Publishers	44th edition, 2018
4	Fast Fourier Transform - Algorithms and Applications	K.R. Rao, Do Nyeon Kim, Jae Jeong Hwang	Springer	1st edition, 2011

SEMESTER S3

SOLID STATE DEVICES

Course Code	**24SJPCECT302**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Mins
Prerequisites (if any)	Physics for Electrical Science (24SJGBPHT121)	**Course Type**	Theory

Course Objectives:

1. This course explains the physical processes and working principles of semiconductor devices, while relating the device performance to material parameters and design criteria.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Review of Semiconductor physics:** Equilibrium and steady state conditions, Concept of effective mass and Fermi level, Density of states & Effective density of states, Equilibrium concentration of electrons and holes. **Carrier transport in semiconductors**: Drift, conductivity and mobility, variation of mobility with temperature and doping, Hall Effect. Diffusion, Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi-Fermi level.	**13**
2	**PN junctions**: Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams, Ideal diode equation. **Bipolar junction transistor**: Transistor action, Base width modulation, Current components in a BJT, Derivation of current components.	**12**
3	**Metal Semiconductor contacts**: Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics. **Ideal MOS capacitor**: band diagrams at equilibrium, accumulation, depletion and inversion, surface potential, CV characteristics, effects of real surfaces, threshold voltage, body effect. MOSFET- Drain current equation of enhancement type MOSFET (derivation)- linear and saturation region, Drain characteristics,	**11**

	transfer characteristics.	

4	**MOSFET scaling**: Need for scaling, constant voltage scaling and constant field scaling. Sub- threshold conduction in MOS. **Short channel effects in MOSFETs**: Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects. **MESFET and FinFET**: Structure, operation and advantages.	**8**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Fermi-Dirac statistics to compute equilibrium carrier concentration, state different carrier transport mechanisms in extrinsic semiconductors and obtain the current densities due to this transport.	**K3**
CO2	Apply the concept of semiconductor physics to solve the current components in semiconductor devices.	**K3**
CO3	Analyze the response of semiconductor devices for different biasing conditions	**K3**
CO4	Outline the effects of scaling in semiconductor devices.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	1	-
CO2	3	2	-	-	-	-	-	-	-	-	2	1	-
CO3	3	2	2	-	-	-	-	-	-	-	2	1	-
CO4	3	2	2	-	-	-	-	-	-	-	2	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Semiconductor device Fundamentals	Robert Pierret	Pearson Education	1/e, 1996
2	Physics of Semiconductor Devices	Michael Shur	Pearson Education	1/e, 2019
3	Semiconductor Physics and Devices, 3ed, An Indian Adaptation	S.M. Sze, M.K. Lee	Wiley	3/e, 2021

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Semiconductor Physics and Devices	Neamen	McGraw Hill	4/e, 2017
2	Physics of Semiconductor Devices	Sze S.M	John Wiley	3/e, 2015
3	Semiconductor Devices: Physics and Technology	Sze S.M	John Wiley	3/e, 2016
4	Operation and Modelling of the MOS Transistor	Yannis Tsividis	Oxford University Press	3/e,2010
5	Semiconductor Physics and Devices, ,	Sze S.M., M.K. Lee,	An Indian Adaptation	3ed, 2021
6	Fundamentals of Semiconductor Devices,	Achuthan, K N Bhat,	McGraw Hill	1e,2015

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117106091
2	https://nptel.ac.in/courses/117106091
3	https://nptel.ac.in/courses/117106091
4	https://nptel.ac.in/courses/117106091

SEMESTER S3

ANALOG CIRCUITS

Course Code	**24SJPCECT303**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Introduction to Electrical and Electronics Engineering (Part 2: Electronics Engineering) 24SJGXEST104	**Course Type**	Theory

Course Objectives:

1. To introduce and verify basic principles, operation and applications of the various analog electronic circuits and devices
2. To understand and analyze the design and working of amplifiers and their configurations.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Wave Shaping Circuits:** RC differentiating and integrating circuits, Transient analysis of RC differentiating and integrating circuits for sinusoidal, step and square inputs. First order low pass and high pass filters & analysis. Diode Clipping and clamping circuits. **BJT/MOSFET Biasing:** Need for biasing, DC load line, operating point, BJT biasing (CE configuration)– fixed bias & voltage divider bias (Design & analysis). MOSFET biasing- fixed bias & voltage divider bias	**10**
2	**BJT Amplifiers:** Design of RC coupled CE amplifier - small signal analysis of CE amplifier using hybrid- π model (low and mid frequency`). The high-frequency hybrid-π model of BJT, Miller effect, High frequency response of single stage CE amplifier, short circuit current gain, cut-off frequency f_β & unity gain bandwidth f_T. **MOSFET Amplifiers:** Design of CS amplifier, Small signal analysis using hybrid- π model (mid frequency only), Small signal voltage gain, input & output	**12**

	impedance, CS stage with current source load and diode connected load. **Multistage BJT Amplifiers:** Types of multistage amplifiers, Effect of cascading on gain and bandwidth. BJT& MOSFET cascode amplifier (circuit diagram and working, analysis not required)	
3	**Feedback amplifiers:** The general feedback structure, Effect of negative feedback on gain, bandwidth, noise reduction and distortion. The four basic feedback topologies, Analysis of discrete BJT circuits in voltage-series and voltage-shunt feedback topologies - voltage gain, input and output impedance. **Oscillators:** Classification, criterion for oscillation, Wien bridge oscillator, Hartley and Crystal oscillator. (Working principle and design equations of the circuits; analysis of Wien bridge oscillator only required).	**11**
4	**Power amplifiers:** Classification, Transformer coupled class A power amplifier, push pull class B and class AB power amplifiers, complementary- symmetry class B and Class AB power amplifiers. **Linear Voltage Regulators:** Types of voltage regulators- series and shunt - working and design, load & line regulation, short circuit protection ,fold back Protection & current boosting.	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Design wave shaping circuits using first order RC network and diodes.	**K3**
CO2	Design single stage and multistage BJT amplifier circuits and MOSFET amplifier circuits using equivalent models.	**K3**
CO3	Apply the working principles of feedback in the design of oscillators and feedback amplifier circuits.	**K3**
CO4	Design power amplifiers and voltage regulator circuits.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	-	2	-	-	-	-	-	2	3	2
CO2	3	3	1	-	2	-	-	-	-	-	2	3	2
CO3	3	3	`2	-	2	-	-	-	-	-	2	3	2
CO4	3	3	2	-	2	-	-	-	-	-	2	3	2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electronic Devices and Circuit Theory.	Robert Boylestad and L Nashelsky	Pearson	11th edition, 2015
2	Microelectronic Circuits	Sedra A. S. and K. C. Smith,	Oxford University Press, 2013	6th edition, 2013
3	Electronic Circuits and Devices	Theodore F. Bogart; Beasley, Jeffrey S.; Guillermo Rico	Pearson Education India	6th edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Microelectronics	Razavi B.	Wiley	2nd edition, 2015
2	Electronic Devices and Circuits	David A Bell	Oxford University Press	5th edition, 2008
3	Electronic Circuits Analysis and Design 1	D. Meganathan	Yes Dee Publishing	1st edition, 2023
4	Analysis and Design of Electronic Circuits	K. Gopakumar	OWL Books	1st edition, 2023

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/108/106/108106188/
2	https://archive.nptel.ac.in/courses/108/106/108106188/
3	https://archive.nptel.ac.in/courses/108/106/108106188/

SEMESTER S3

LOGIC CIRCUIT DESIGN

Course Code	**24SJPBECT304**	**CIE Marks**	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	**ESE Marks**	40
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	24SJGXEST104 Introduction to Electrical & Electronics Engineering	**Course Type**	Theory

Course Objectives:

1. To understand the number systems in digital systems
2. To introduce the basic postulates of Boolean algebra, digital logic gates and Boolean expressions
3. To design and implement combinational and sequential circuits.
4. To design and implement digital circuits using Hardware Descriptive Language like Verilog on FPGA

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to digital circuits:** Review of number systems representation-conversions, Arithmetic of Binary number systems, Signed and unsigned numbers,BCD **Boolean algebra:** Theorems, sum of product and product of sum - simplification, canonical forms- min term and max term, Simplification of Boolean expressions - Karnaugh map (upto 4 variables), Implementation of Boolean expressions using universal gates.	**9**
2	**Combinational logic circuits**- Half adder and Full adders, Subtractors, BCD adder, Ripple carry and carry look ahead adders, Decoders, Encoders, Code converters, Comparators, Parity generator, Multiplexers, De-multiplexers, Implementation of Boolean algebra using MUX.	**9**

3	**Sequential Circuits:** SR Latch, Flip flops - SR, JK, Master-Slave JK, D and T Flip flops. Conversion of Flip flops, Excitation table and characteristic equation. Design of Asynchronous, Synchronous and Mod N counters.	**9**
4	Shift registers-SIPO, SISO, PISO, PIPO and Universal shift registers. Ring and Johnsons counters. **Logic Families:** -Electrical characteristics of logic gates (Noise margin, Fan- in, Fan-out, Propagation delay, Transition time, Power -delay product) -TTL, ECL, CMOS.Circuit description and working of TTL and CMOS inverter, CMOS NAND and CMOS NOR gates.	**9**

Suggestion on Project Topics

- A random sequence generator
- Traffic light controller
- Multiplexer based person priority check in system at airport
- Waveform generator
- Object/Visitor counter
- Fast adders
- Hamming code-based parity checker
- Arithmetic Logic Unit using FPGA

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**30**	**12.5**	**12.5**	**60**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16marks)**	• Each question carries 6 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 2 sub divisions. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Understand fundamental concepts of digital representation of information and Boolean algebra to deduce optimal digital circuits.	**K2**
CO2	Design and implement combinational logic circuits.	**K3**
CO3	Design and implement sequential logic circuits.	**K3**
CO4	Outline the performance of logic families with Respect to different parameters.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	2	-	-	-	-	-	-	3	1	1
CO2	3	3	3	3	3	3	3	3	-	-	3	3	1
CO3	3	3	3	3	3	3	3	3	-	-	3	3	1
CO4	3		2	-	-	-	-	-	-	-	3	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Fundamentals	Thomas L. Floyd	Pearson Education	11th Edition, 2017
2	Fundamentals of Digital Logic with Verilog Design	Stephen Brown	McGraw Hill Education	2nd Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog	M Morris Mano, Michael D. Ciletti	Pearson India	6th Edition, 2018
2	Fundamentals of Digital Circuits	A. Ananthakumar	PHI	4th Edition, 2016
3	Introduction to Logic Circuits & Logic Design with Verilog	Brock J. LaMeres	Springer	2nd Edition, 2019
4	Digital Design Verilog HDL and Fundamentals	Joseph Cavanagh	CRC Press	1st Edition, 2008
5	Digital Circuits and Systems	D.V. Hall	Tata McGraw Hill	1989

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
2	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
3	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/
4	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/

PBL Course Elements

L: Lecture (3 Hrs.)	R: Project (1 Hr.), 2 Faculty Members		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation / Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	**10**
2	Execution and Implementation	**10**
3	Final Presentations and report	**10**
Total		**30**

Project Assessment and Evaluation criteria (30 Marks)

1. **Project Planning and Proposal (5 Marks)**

- Clarity and feasibility of the project plan
- Research and background understanding
- Defined objectives and methodology

2. **Contribution in Progress Presentation and Question Answer Sessions (4 Marks)**

- Individual contribution to the presentation
- Effectiveness in answering questions and handling feedback

3. **Involvement in the Project Work and Team Work (3 Marks)**

- Active participation and individual contribution
- Teamwork and collaboration

4. **Execution and Implementation (10 Marks)**

- Adherence to the project timeline and milestones
- Application of theoretical knowledge and problem-solving
- Final Result

5. **Final Presentation (5 Marks)**

- Quality and clarity of the overall presentation
- Individual contribution to the presentation
- Effectiveness in answering questions

6. **Project Quality, Innovation, and Creativity (3 Marks)**

- Overall quality and technical excellence of the project
- Innovation and originality in the project
- Creativity in solutions and approaches

SEMESTER S3

INTRODUCTION TO ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

Course Code	**24SJGNEST305**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Demonstrate a solid understanding of advanced linear algebra concepts, machine learning algorithms and statistical analysis techniques relevant to engineering applications, principles and algorithms.
2. Apply theoretical concepts to solve practical engineering problems, analyze data to extract meaningful insights, and implement appropriate mathematical and computational techniques for AI and data science applications.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to AI and Machine Learning**: Basics of Machine Learning - Supervised Learning, Unsupervised Learning, Reinforcement Learning (Basics only) -types of Machine Learning systems-challenges in ML- Supervised learning model example- regression models- Classification model example- Logistic regression-unsupervised model example- K-means clustering. Artificial Neural Network- Perceptron- Universal Approximation Theorem (statement only)- Multi-Layer Perceptron- Deep Neural Network (definition only)- demonstration of regression and classification problems using MLP. (Text-2)	**11**
2	**Mathematical Foundations of AI and Data science**: Role of linear algebra in Data representation and analysis - Vectors, Matrices, Matrix Multiplication and Transformation – Matrix decomposition- Singular Value Decomposition (SVD)- Spectral decomposition- Dimensionality reduction technique- Principal Component Analysis (PCA). (Text-1)	**11**

3	**Applied Probability and Statistics for AI and Data Science**: Basics of probability- Sample Space, Event, Probability of an Event - random variables and statistical measures - rules in probability- Addition rule, Multiplication rule, Complementary rule - Bayes theorem and its applications- statistical estimation-Maximum Likelihood Estimator (MLE) - statistical summaries- Correlation analysis- linear correlation (direct problems only)- regression analysis- linear regression (using least square method) (Text book 4)	**11**
4	**Basics of Data Science**: Benefits of data science-use of statistics and Machine Learning in Data Science- data science process - applications of Machine Learning in Data Science- modelling process- demonstration of ML applications in data science- Big Data and Data Science. (For visualization the software tools like Tableau, PowerBI, R or Python can be used. For Machine Learning implementation, Python, MATLAB or R can be used.)(Text book-5)	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply the concept of machine learning algorithms including neural networks and supervised/unsupervised learning techniques for engineering applications.	**K3**
CO2	Apply advanced mathematical concepts such as matrix operations, singular values, and principal component analysis to analyze and solve engineering problems**.**	**K3**
CO3	Analyze and interpret data using statistical methods including descriptive statistics, correlation, and regression analysis to derive meaningful insights and make informed decisions.	**K3**
CO4	Integrate statistical approaches and machine learning techniques to ensure practically feasible solutions in engineering contexts.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	3	3	-	-	-	-	-	-	-	1	-
CO2	3	3	3	3	-	-	-	-	-	-	-	1	-
CO3	3	3	3	3	-	-	-	-	-	-	-	-	-
CO4	3	3	3	3	-	-	-	-	-	-	-	1	1

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to Linear Algebra	Gilbert Strang	Wellesley-Cambridge Press	6th edition, 2023
2	Hands-on machine learning with Scikit-Learn, Keras, and TensorFlow	Aurélien Géron	O'Reilly Media, Inc.	2nd edition,2022
3	Mathematics for machine learning	Deisenroth, Marc Peter, A. Aldo Faisal, and Cheng Soon Ong	Cambridge University Press	1st edition. 2020
4	Fundamentals of mathematical statistics	Gupta, S. C., and V. K. Kapoor	Sultan Chand & Sons	9th edition, 2020
5	Introducing data science: big data, machine learning, and more, using Python tools	Cielen, Davy, and Arno Meysman	Simon and Schuster	1st edition, 2016

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Data science: concepts and practice	Kotu, Vijay, and Bala Deshpande	Morgan Kaufmann	2nd edition, 2018
2	Probability and Statistics for Data Science	Carlos Fernandez-Granda	Center for Data Science in NYU	1st edition, 2017
3	Foundations of Data Science	Avrim Blum, John Hopcroft, and Ravi Kannan	Cambridge University Press	1st edition, 2020
4	Statistics For Data Science	James D. Miller	Packt Publishing	1st edition, 2019
5	Probability and Statistics -The Science of Uncertainty	Michael J. Evans and Jeffrey S. Rosenthal	University of Toronto	1st edition, 2009
6	An Introduction to the Science of Statistics: From Theory to Implementation	Joseph C. Watkins	chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.math.arizo	Preliminary Edition.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/106/106106198/
2	https://archive.nptel.ac.in/courses/106/106/106106198/ https://ocw.mit.edu/courses/18-06-linear-algebra-spring-2010/resources/lecture-29-singular- value-decomposition/
3	https://ocw.mit.edu/courses/18-650-statistics-for-applications-fall-2016/resources/lecture-19- video/
4	https://archive.nptel.ac.in/courses/106/106/106106198/

SEMESTER S3/S4

ECONOMICS FOR ENGINEERS

Course Code	24SJICHUT346	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Understanding of finance and costing for engineering operation, budgetary planning and control
2. Provide fundamental concept of micro and macroeconomics related to engineering industry
3. Deliver the basic concepts of Value Engineering.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Basic Economics Concepts - Basic economic problems – Production Possibility Curve – Utility – Law of diminishing marginal utility – Law of Demand - Law of supply – Elasticity - measurement of elasticity and its applications – Equilibrium- Changes in demand and supply and its effects Production function - Law of variable proportion – Economies of Scale – Internal and External Economies – Cobb-Douglas Production Function	6
2	Cost concepts – Social cost, private cost – Explicit and implicit cost – Sunk cost - Opportunity cost - short run cost curves - Revenue concepts Firms and their objectives – Types of firms – Markets - Perfect Competition – Monopoly - Monopolistic Competition - Oligopoly (features and equilibrium of a firm)	6

3	Monetary System – Money – Functions - Central Banking – Inflation - Causes and Effects – Measures to Control Inflation - Monetary and Fiscal policies – Deflation Taxation – Direct and Indirect taxes (merits and demerits) - GST National income – Concepts - Circular Flow – Methods of Estimation and Difficulties - Stock Market – Functions- Problems faced by the Indian stock market-Demat Account and Trading Account – Stock market Indicators- SENSEX and NIFTY	6
4	Value Analysis and value Engineering - Cost Value, Exchange Value, Use Value, Esteem Value - Aims, Advantages and Application areas of Value Engineering - Value Engineering Procedure - Break-even Analysis - Cost-Benefit Analysis - Capital Budgeting - Process planning	6

Course Assessment Method

(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Case study/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
10	15	12.5	12.5	50

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
Minimum 1 and Maximum 2 Questions from each module. Total of 6 Questions, each carrying 3 marks (6x3 =18marks)	2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 2 sub divisions. Each question carries 8 marks. (4x8 = 32 marks)	50

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the fundamentals of various economic issues using laws and learn the concepts of demand, supply, elasticity and production function.	**K2**
CO2	Develop decision making capability by applying concepts relating to costs and revenue, and acquire knowledge regarding the functioning of firms in different market situations.	**K3**
CO3	Outline the macroeconomic principles of monetary and fiscal systems, national income and stock market.	**K2**
CO4	Make use of the possibilities of value analysis and engineering, and solve simple business problems using break even analysis, cost benefit analysis and capital budgeting techniques.	**K3**

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	-	-	-	-	-	1	-	-	-	-	1
CO2	-	-	-	-	-	1	1	-	-	-	1
CO3	-	-	-	-	1	-	-	-	-	-	2
CO4	-	-	-	-	1	1	-	-	-	-	2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Managerial Economics	Geetika, Piyali Ghosh and Chodhury	Tata McGraw Hill,	2015
2	Engineering Economy	H. G. Thuesen, W. J. Fabrycky	PHI	1966
3	Engineering Economics	R. Paneerselvam	PHI	2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Engineering Economy	Leland Blank P.E, Anthony Tarquin P. E.	Mc Graw Hill	7TH Edition
2	Indian Financial System	Khan M. Y.	Tata McGraw Hill	2011
3	Engineering Economics and analysis	Donald G. Newman, Jerome P. Lavelle	Engg. Press, Texas	2002
4	Contemporary Engineering Economics	Chan S. Park	Prentice Hall of India Ltd	2001

SEMESTER S3/S4

ENGINEERING ETHICS AND SUSTAINABLE DEVELOPMENT

Course Code	**24SJICHUT347**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	2:0:0:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. Equip with the knowledge and skills to make ethical decisions and implement gender-sensitive practices in their professional lives.
2. Develop a holistic and comprehensive interdisciplinary approach to understanding engineering ethics principles from a perspective of environment protection and sustainable development.
3. Develop the ability to find strategies for implementing sustainable engineering solutions.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Fundamentals of ethics** - Personal vs. professional ethics, Civic Virtue, Respect for others, **Profession and Professionalism,** Ingenuity, diligence and responsibility, Integrity in design, development, and research domains, Plagiarism, a balanced outlook on law - challenges - case studies, **Technology and digital revolution**-Data, information, and knowledge, Cybertrust and cybersecurity, Data collection & management, **High technologies: connecting people and places**-accessibility and social impacts, **Managing conflict**, Collective bargaining, **Confidentiality**, Role of confidentiality in moral integrity, **Codes of Ethics**. **Basic concepts in Gender Studies** - sex, gender, sexuality, gender spectrum: beyond the binary, gender identity, gender expression, gender stereotypes, **Gender disparity and discrimination in education**,	**6**

	employment and everyday life, History of women in Science & Technology, Gendered technologies & innovations**, Ethical values and practices in connection with gender** - equity, diversity & gender justice, **Gender policy and women/transgender empowerment initiatives.**	
2	**Introduction to Environmental Ethics:** Definition, importance and historical development of environmental ethics, key philosophical theories (anthropocentrism, biocentrism, ecocentrism). **Sustainable Engineering Principles:** Definition and scope, triple bottom line (economic, social and environmental sustainability), life cycle analysis and sustainability metrics. **Ecosystems and Biodiversity:** Basics of ecosystems and their functions, Importance of biodiversity and its conservation, Human impact on ecosystems and biodiversity loss, An overview of various ecosystems in Kerala/India, and its significance. **Landscape and Urban Ecology:** Principles of landscape ecology, Urbanization and its environmental impact, Sustainable urban planning and green infrastructure.	**6**
3	**Hydrology and Water Management:** Basics of hydrology and water cycle, Water scarcity and pollution issues, Sustainable water management practices, Environmental flow, disruptions and disasters. **Zero Waste Concepts and Practices:** Definition of zero waste and its principles, Strategies for waste reduction, reuse, reduce and recycling, Case studies of successful zero waste initiatives. **Circular Economy and Degrowth:** Introduction to the circular economy model, Differences between linear and circular economies, degrowth principles, Strategies for implementing circular economy practices and degrowth principles in engineering. **Mobility and Sustainable Transportation:** Impacts of transportation on the environment and climate, Basic tenets of a Sustainable Transportation design, Sustainable urban mobility solutions, Integrated mobility systems, E-Mobility, Existing and upcoming models of sustainable mobility solutions.	**6**
	Renewable Energy and Sustainable Technologies: Overview of renewable energy sources (solar, wind, hydro, biomass), Sustainable technologies in energy production and consumption, Challenges and	

4	opportunities in renewable energy adoption. **Climate Change and Engineering Solutions:** Basics of climate change science, Impact of climate change on natural and human systems, Kerala/India and the Climate crisis, Engineering solutions to mitigate, adapt and build resilience to climate change. **Environmental Policies and Regulations:** Overview of key environmental policies and regulations (national and international), Role of engineers in policy implementation and compliance, Ethical considerations in environmental policy-making. **Case Studies and Future Directions:** Analysis of real- world case studies, Emerging trends and future directions in environmental ethics and sustainability, Discussion on the role of engineers in promoting a sustainable future.	**6**

Course Assessment Method

(CIE: 50 marks , ESE: 50)

Continuous Internal Evaluation Marks (CIE):

Continuous internal evaluation will be based on individual and group activities undertaken throughout the course and the portfolio created documenting their work and learning. The portfolio will include reflections, project reports, case studies, and all other relevant materials.

- The students should be grouped into groups of size 4 to 6 at the beginning of the semester. These groups can be the same ones they have formed in the previous semester.
- Activities are to be distributed between 2 class hours and 3 Self-study hours.
- The portfolio and reflective journal should be carried forward and displayed during the 7th Semester Seminar course as a part of the experience sharing regarding the skills developed through various courses.

Sl. No.	Item	Particulars	Group/Individual (G/I)	Marks
1	Reflective	Weekly entries reflecting on what was learned, personal insights, and how it can be applied to local contexts.	I	5
2	Micro project (Detailed documentation of the project, including methodologies, findings, and reflections)	1 a) Perform an Engineering Ethics Case Study analysis and prepare a report 1 b) Conduct a literature survey on 'Code of Ethics for Engineers' and prepare a sample code of ethics	G	8
		2. Listen to a TED talk on a Gender-related topic, do a literature survey on that topic and make a report citing the relevant papers with a specific analysis of the Kerala context	G	5
		3. Undertake a project study based on the concepts of sustainable development* - Module II, Module III & Module IV	G	12
3	Activities	2. One activity* each from Module II, Module III & Module IV	G	15
4	Final Presentation	A comprehensive presentation summarising the key takeaways from the course, personal reflections, and proposed future actions based on the learnings.	G	5
		Total Marks		**50**

*Can be taken from the given sample activities/projects

Evaluation Criteria:

- **Depth of Analysis**: Quality and depth of reflections and analysis in project reports and case studies.
- **Application of Concepts**: Ability to apply course concepts to real-world problems and local contexts.
- **Creativity**: Innovative approaches and creative solutions proposed in projects and reflections.
- **Presentation Skills**: Clarity, coherence, and professionalism in the final presentation.

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Develop the ability to apply the principles of engineering ethics in their professional life.	**K3**
CO2	Develop the ability to exercise gender-sensitive practices in their professional lives	**K4**
CO3	Develop the ability to explore contemporary environmental issues and sustainable practices.	**K5**
CO4	Develop the ability to analyse the role of engineers in promoting sustainability and climate resilience.	**K4**
CO5	Develop interest and skills in addressing pertinent environmental and climate-related challenges through a sustainable engineering approach.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	-	-	-	-	-	✓	✓	✓	✓	-	✓
CO2	-	✓	-	-	-	✓	✓	✓	✓	-	✓
CO3	-		-	-	-	✓	✓	✓	✓	-	✓
CO4	-	✓	-	-	-	✓	✓	✓	✓	-	✓
CO5	-	-	-	-	-	✓	✓	✓	✓	-	✓

*As this is a common course, the mapping will be decided in the concerned course committee.

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Ethics in Engineering Practice and Research	Caroline Whitbeck	Cambridge University Press & Assessment	2nd edition & August 2011
2	Virtue Ethics and Professional Roles	Justin Oakley	Cambridge University Press & Assessment	November 2006
3	Sustainability Science	Bert J. M. de Vries	Cambridge University Press & Assessment	2nd edition & December 2023
4	Sustainable Engineering Principles and Practice	Bhavik R. Bakshi,	Cambridge University Press & Assessmen	2019
5	Engineering Ethics	M Govindarajan, S Natarajan and V S Senthil Kumar	PHI Learning Private Ltd, New Delhi	2012
6	Professional ethics and human values	RS Naagarazan	New age international (P) limited New Delhi	2006.
7	Ethics in Engineering	Mike W Martin and Roland Schinzinger,	Tata McGraw Hill Publishing Company Pvt Ltd, New Delhi	4" edition, 2014

Suggested Activities/Projects:

Module-II

- Write a reflection on a local environmental issue (e.g., plastic waste in Kerala backwaters or oceans) from different ethical perspectives (anthropocentric, biocentric, ecocentric).
- Write a life cycle analysis report of a common product used in Kerala (e.g., a coconut, bamboo or rubber-based product) and present findings on its sustainability.
- Create a sustainability report for a local business, assessing its environmental, social, and economic impacts
- Presentation on biodiversity in a nearby area (e.g., a local park, a wetland, mangroves, college campus etc) and propose conservation strategies to protect it.
- Develop a conservation plan for an endangered species found in Kerala.
- Analyze the green spaces in a local urban area and propose a plan to enhance urban ecology using native plants and sustainable design.
- Create a model of a sustainable urban landscape for a chosen locality in Kerala.

Module-III

- Study a local water body (e.g., a river or lake) for signs of pollution or natural flow disruption and suggest sustainable management and restoration practices.
- Analyse the effectiveness of water management in the college campus and propose improvements - calculate the water footprint, how to reduce the footprint, how to increase supply through rainwater harvesting, and how to decrease the supply-demand ratio
- Implement a zero-waste initiative on the college campus for one week and document the challenges and outcomes.
- Develop a waste audit report for the campus. Suggest a plan for a zero-waste approach.
- Create a circular economy model for a common product used in Kerala (e.g., coconut oil, cloth etc).
- Design a product or service based on circular economy and degrowth principles and present a business plan.
- Develop a plan to improve pedestrian and cycling infrastructure in a chosen locality in Kerala

Module-IV

- Evaluate the potential for installing solar panels on the college campus including cost- benefit analysis and feasibility study.
- Analyse the energy consumption patterns of the college campus and propose sustainable alternatives to reduce consumption - What gadgets are being used? How can we reduce demand using energy- saving gadgets?
- Analyse a local infrastructure project for its climate resilience and suggest improvements.
- Analyse a specific environmental regulation in India (e.g., Coastal Regulation Zone) and its impact on local communities and ecosystems.
- Research and present a case study of a successful sustainable engineering project in Kerala/India (e.g., sustainable building design, water management project, infrastructure project).
- Research and present a case study of an unsustainable engineering project in Kerala/India highlighting design and implementation faults and possible corrections/alternatives (e.g., a housing complex with water logging, a water management project causing frequent floods, infrastructure project that affects surrounding landscapes or ecosystems).

SEMESTER S3

ANALOG CIRCUITS LAB

Course Code	**24SJPCECL307**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Basic Electrical and Electronics Engineering Workshop (24SJGXESL106)	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the analog circuits design using discrete components.
2. Familiarise the students with simulation of basic analog circuits

Expt. No.	**Experiments**
Part A – List of Experiments using discrete components (Any *Six* experiments mandatory)	
1	RC Integrating and Differentiating Circuits – (Transient analysis with different inputs and frequency response)
2	Diode Clipping and Clamping Circuits (Transient and transfer characteristics)
3	CE amplifier – Design for a specific voltage gain and plot frequency response characteristics
4	CS MOSFET amplifier - Design for a specific voltage gain and plot frequency response characteristics
5	Cascaded amplifier (CE – CE) - Design for a specific voltage gain and plot frequency response characteristics
6	Cascode amplifier - Design for a specific voltage gain and plot frequency response characteristics

7	Feedback amplifiers (current series & voltage series) - Design for a specific voltage gain and plot frequency response characteristics
8	RC oscillators – RC phase shift or Wien bridge oscillator
9	Power amplifiers (Transformer less) – Class B & Class AB

10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).
Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Open-Source Tools such as QUCS, KiCad, LT SPICE, or variants of SPICE tools.	
1	RC Integrating and Differentiating Circuits – (Transient analysis with different inputs and frequency response)
2	Diode Clipping and Clamping Circuits (Transient and transfer characteristics)
3	CE amplifier – Design for a specific voltage gain and plot frequency response characteristics
4	CS MOSFET amplifier - Design for a specific voltage gain and plot frequency response characteristics
5	Cascaded amplifier (CE – CE) - Design for a specific voltage gain and plot frequency response characteristics
6	Cascode amplifier - Design for a specific voltage gain and plot frequency response characteristics
7	Feedback amplifiers (current series & voltage series) - Design for a specific voltage gain and plot frequency response characteristics
8	RC oscillators – RC phase shift or wien bridge oscillator
9	Power amplifiers (Transformer less) – Class B & Class AB
10	Transistor series voltage regulator – Design for a specific output voltage with & without short circuit protection (plot load & line regulation characteristics).

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- **Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.**
  - ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of basic analog circuits using discrete components.	**K3**
CO2	Design and simulate the functioning of basic analog circuits using simulation tools	**K3**
CO3	Conduct troubleshooting of a given circuit and to analyze it as a team	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	-	-	-	-	3	-	-	3	2	-
CO2	3	2	2	-	3	-	-	3	-	-	3	2	3
CO3	3	2	2	-	-	-	-	3	-	-	3	1	-

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Electronic Devices and Circuits	David A Bell	Oxford University Press, 2008	5th edition
2	Electronic Circuits Analysis and Design 1	D. Meganathan	Yes Dee Publishing, 2023	1st edition

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**

   - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
   - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. **Conduct of Experiments (7 Marks)**

   - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
   - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
   - Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

   - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
   - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

   - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

   - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
   - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
   - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
   - Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

   - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and Result with Valid Inference/Quality of Output (10 Marks)

   - Accuracy of Results: Precision and correctness of the obtained results.
   - Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

3. **Viva Voce (10 Marks)**

   - Ability to explain the experiment, procedure results and answer related questions
   - Proficiency in answering questions related to theoretical and practical aspects of the subject.

4. **Record (5 Marks)**

   - Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S3

LOGIC CIRCUIT DESIGN LAB

Course Code	**24SJPCECL308**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the Digital Logic Design through the implementation of Logic Circuits.
2. Familiarise the students with the HDL based Digital Design and FPGA boards

Expt. No.	Experiments
Part A – List of Experiments using digital components (Any *Six* experiments mandatory)	
1	Realization of functions using basic and universal gates (SOP and POS forms).
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	4 bit adder/subtractor and BCD adder using 7483
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Asynchronous Counter : 3 bit up/down counter, Realization of Mod N Counter
6	Synchronous Counter: Realization of 4-bit up/down counter, Realization of Mod-N counters
7	Ring counter and Johnson Counter.
8	Realization of counters using IC's (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)
10	Sequence Generator / Detector

Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Verilog and implementation using small FPGA	
1	Experiment 1:Introduction to Verilog & Familiarization of Logic gates on FPGA (a) Familiarization of a small FPGA board and its ports and interface. (b) Create the .pcf files for your FPGA board. (c) Familiarization of the basic syntax of verilog Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables. (e) Verify the universality and non associativity of NAND and NOR gates by uploading the corresponding verilog files to the FPGA boards.
2	Experiment 2: Adders in Verilog (a) Development of verilog modules for half adder in any of the 3 modeling styles (b) Development of verilog modules for full adder in structural modeling using half adder.
3	Experiment 3: Mux and Demux in Verilog (a) Development of verilog modules for a 4x1 MUX. (b) Development of verilog modules for a 1x4 DEMUX.
4	Experiment 4: Flipflops and counters (a) Development of verilog modules for SR, JK and D flipflops. (b) Development of verilog modules for a binary decade/Johnson/Ring counters
5	Experiment 5. Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function
6	Experiment 6. Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D
7	Experiment 7: Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.
8	Experiment 8: Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.

9	Experiment 9. BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use ouput ports for connection to the display.

Course Assessment Method

(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs	**K3**
CO2	Apply an industry compatible hardware description language to implement digital circuits	**K3**
CO3	Implement digital circuits on FPGA boards and connect external hardware to the boards	**K3**
CO4	Function effectively as an individual and in a team to accomplish the given task.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO12	PSO1	PSO2
CO1	3	3	3	2	3	-	-	3	-	-	3	2	2
CO2	3	1	1	3	3	-	-	3	-	1	3	2	2
CO3	3	1	1	3	3	-	-	3	-	1	3	2	2
CO4	3	3	3	-	3	-	-	3	-	-	3	-	-

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL Synthesis: A Practical Primer	J. Bhasker	B. S. Publications,	2001
2	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009	5th Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL :A guide to digital design and synthesis	Palnitkar S.	Prentice Hall; 2003.	2nd Edn.,

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. **Lab Reports and Record Keeping (6 Marks)**

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

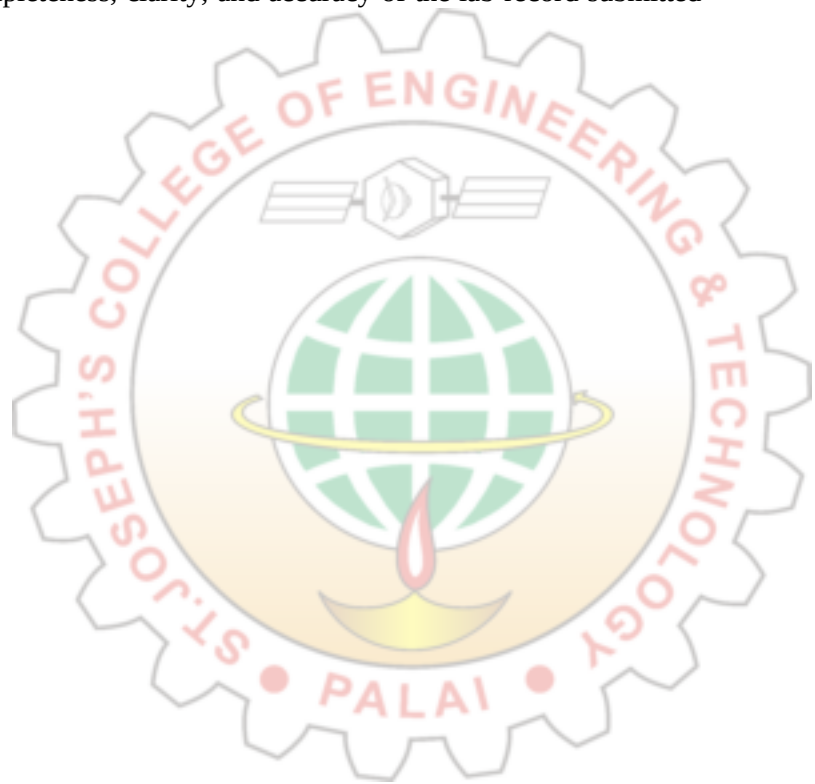
- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

Completeness, clarity, and accuracy of the lab record submitted




ST.JOSEPH'S COLLEGE OF ENGINEERING & TECHNOLOGY
PALAI

Department of Electronics and Communication Engineering

ST. JOSEPH'S
COLLEGE OF ENGINEERING
AND TECHNOLOGY,
- PALAI -
AUTONOMOUS

Syllabus - Fourth Semester

FOURTH SEMESTER (January-June)														
Sl. No:	Slot	Course Code	Course Type	Course Category	Course Title (Course Name)	Credit Structure				SS	Total Marks		Credits	Hrs./ Week
						L	T	P	R		CIE	ESE		
1	A	24SJGBMAT401	BSC	GC	Mathematics for Electrical Science - 4	3	0	0	0	4.5	40	60	3	3
2	B	24SJPCECT402	PC	PC	Signals and Systems	3	1	0	0	5	40	60	4	4
3	C	24SJPCECT403	PC	PC	Linear Integrated Circuits	3	1	0	0	5	40	60	4	4
4	D	24SJPBECT404	PC-PBL	PB	Microcontrollers	3	0	0	1	5.5	60	40	4	4
5	E	24SJPEECT41N	PE	PE	Program Elective-1	3	0	0	0	4.5	40	60	3	3
6	G S3/S4	24SJICHUT346 24SJICHUT347	HMC	IC	Economics for Engineers Engineering Ethics and Sustainable Development	2	0	0	0	3	50	50	2	2
7	L	24SJPCECL407	PCL	PC	Linear Integrated Circuits Lab	0	0	3	0	1.5	50	50	2	3
8	Q	24SJPCECL408	PCL	PC	Microcontroller Lab	0	0	3	0	1.5	50	50	2	3
9	R/M/H		VAC		Remedial/Minor/Honours Course	3	1	0	0	5			4*	4*
Total										**31/36**			**24/28***	**26/30***

SEMESTER S4

MATHEMATICS FOR ELECTRICAL SCIENCE– 4

(B Group)

Course Code	**24SJGBMAT401**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Basic calculus	**Course Type**	Theory

Course Objectives:

1. To familiarize students with the foundations of probabilistic and statistical analysis mostly used in varied applications in engineering and science.
2. To expose the students to the basics of random processes, which will be essential for their subsequent study of analog and digital communication.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Random variables, Discrete random variables and their probability distributions, Cumulative distribution function, Expectation, Mean and variance, Binomial distribution, Poisson distribution, Poisson distribution as a limit of the binomial distribution, Joint probability mass function of two discrete random variables, Marginal probability mass function, Independent random variables, Expected value of a function of two discrete variables. **[Text 1: Relevant topics from sections 3.1 to 3.4, 3.6, 5.1, 5.2]**	**9**
2	Continuous random variables and their probability distributions, Cumulative distribution function, Expectation, Mean and variance, Uniform, Normal and Exponential distributions, Joint pdf of two Continuous random variables, Marginal pdf, Independent random variables, Expectation value of a function of two continuous variables. **[Text 1: Relevant topics from sections 3.1, 4.1, 4.2, 4.3, 4.4, 5.1, 5.2]**	**9**

3	Confidence Intervals, Confidence Level, Confidence Intervals, and One-sided confidence intervals for a Population Mean for large and small samples (normal distribution and *t*-distribution), Hypotheses and Test Procedures, Type I and Type II errors, z-Tests for Hypotheses about a Population Mean (for a large sample), *t*-Test for Hypotheses about a Population Mean (for a small sample), and Tests concerning a population proportion for large and small samples. **[Text 1: Relevant topics from 7.1, 7.2, 7.3, 8.1, 8.2, 8.3, 8.4]**	**9**
4	Random process concept, classification of process, Methods of Description of Random process, Special classes, Average Values of Random Process, Stationarity- SSS, WSS, Autocorrelation functions and its properties, Ergodicity, Mean-Ergodic Process, Mean-Ergodic Theorem, Correlation Ergodic Process, Distribution Ergodic Process. **[Text 2: Relevant topics from Chapter 6]**	**9**

Course Assessment Method

(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub-divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Understand the concepts, properties, and important models of discrete random variables and apply them to suitable random phenomena.	**K3**
CO2	Understand the concepts, properties, and important models of continuous random variables and apply them to suitable random phenomena.	**K3**
CO3	Estimate population parameters, assess their certainty with confidence intervals, and test hypotheses about population means and proportions using *z*-tests and the one-sample *t*-test.	**K3**
CO4	Analyze random processes by classifying them, describing their properties, utilizing autocorrelation functions, and understanding their applications in signal processing and communication systems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	2	2	-	-	-	-	-	-	2
CO2	3	3	2	2	-	-	-	-	-	-	2
CO3	3	3	2	2	-	-	-	-	-	-	2
CO4	3	3	2	2	-	-	-	-	-	-	2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Probability and Statistics for Engineering and the Sciences	Devore J. L	Cengage Learning	9th edition, 2016
2	Probability, Statistics and Random Processes	T Veerarajan	The McGraw-Hill	3rd edition, 2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Probability, Random Variables and Stochastic Processes,	Papoulis, A. & Pillai, S.U.,	McGraw Hill.	4th edition, 2002
2	Introduction to Probability and Statistics for Engineers and Scientists	Ross, S. M.	Academic Press	6th edition, 2020
3	Probability and Random Processes	Palaniammal, S.	PHI Learning Private Limited	3rd edition, 2015
4	Introduction to Probability	David F. Anderson, Timo, Benedek	Cambridge	1st edition, 2017

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1,2,4	https://archive.nptel.ac.in/courses/117/105/117105085/

SEMESTER S4

SIGNALS AND SYSTEMS

Course Code	**24SJPCECT402**	**CIE Marks**	**40**
Teaching Hours/Week (L: T:P: R)	**3:1:0:0**	**ESE Marks**	**60**
Credits	**4**	**Exam Hours**	**2 Hrs. 30 Min.**
Prerequisites (if any)	**Mathematics for Electrical and Physical Sciences (24SJGYMAT101, 24SJGYMAT201)**	**Course Type**	**Theory**

Course Objectives:

1. To provide sufficient understanding of different types of signals and systems in time and frequency domain.
2. Analyze LTI systems in time and frequency domain using different transforms

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to signals and systems:** Continuous time and discrete time signals - Elementary signals, Classification of signals, Basic signal operations. Continuous time and discrete time systems – Representation and Classification (memory, causal, stable, linear, time-invariant) Convolution integral and convolution sum operations. Continuous time and discrete time LTI systems-Stability and causality of LTI systems.	**11**
2	**Frequency domain representation of continuous time signals:** Continuous time Fourier series - Exponential Fourier series representation of periodic signals. Continuous time Fourier transform - Convergence and Gibbs phenomenon, Continuous time Fourier transform of standard signals, Properties of Continuous time Fourier transform, Inverse Transform. Bilateral Laplace Transform, Concept of ROC, Relation of Laplace transform to Fourier Transform.	**11**

3	**Sampling of continuous time signals to discrete signals and frequency domain representation of discrete time signals:** Conversion of continuous time signal to discrete time signal, Sampling theorem for low pass signals, Nyquist criteria, Aliasing. Discrete time Fourier transform (DTFT)- DTFT of standard signals, Properties of DTFT, Inverse transform. Z transform- ROC, Properties (Proof not needed), Inverse transform, Relation between DTFT and Z-Transform.	**11**
4	**Analysis of LTI systems using Transforms** Concept of transfer function-Frequency response, Magnitude response and phase response. Analysis of Continuous time LTI systems using Laplace and Fourier transforms. Analysis of discrete time LTI systems using DTFT and Z transforms, Stability and causality using Z transform.	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Classify continuous and discrete time signals and systems based on their properties and perform basic operations on signals.	**K2**
CO2	Apply Fourier and Laplace transforms to represent and analyze continuous time signals in the frequency domain.	**K3**
CO3	Apply the concepts of sampling and use DTFT and Z-transform to represent discrete signals in the frequency domain.	**K3**
CO4	Demonstrate how transforms are used to interpret the frequency response and behavior of LTI systems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	3	-	1	-	-	-	-	-	2	1	-
CO2	3	3	3	-	1	-	-	-	-	-	2	1	-
CO3	3	3	3	-	1	-	-	-	-	-	2	1	-
CO4	3	3	3	-	1	-	-	-	-	-	2	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Signals and Systems	Alan V. Oppenheim and Alan Willsky	Pearson	2/e, 2015
2	Signals and Systems	Simon Haykin	John Wiley	2/e, 2021

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Signals and Systems	Anand Kumar	PHI	3/e, 2013
2	Principles of Signal Processing & Linear systems	B P. Lathi	Oxford University Press	2/e, 2009
3	Signals & Systems - Continuous and Discrete	Rodger E. Ziemer	Pearson	4/e, 2013
4	Analog and Digital Signal Processing	Ashok Ambardar	Brooks/Cole Publishing Company	2/e, 2013
5	Signals and systems - Principles and Applications	Shaila Dinkar Apte	Cambridge University Press	1/e, 2016

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1,2,3,4	https://nptel.ac.in/courses/117101055 https://nptel.ac.in/courses/117104074 https://nptel.ac.in/courses/108104100

SEMESTER S4

LINEAR INTEGRATED CIRCUITS

Course Code	24SJPCECT403	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	Analog Circuits (24SJPCECT303)	Course Type	Theory

Course Objectives:

1. To develop skills to design and analyze circuits using operational amplifiers for various applications.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Differential Amplifiers:** Differential amplifier configurations using BJT, DC Analysis - transfer characteristics; AC analysis - differential and common mode gains, CMRR, input and output resistance, voltage gain, constant current bias, constant current source. **Concept of current mirror**: two-transistor current mirror, Wilson and Widlar current mirrors. **Operational amplifiers (Op Amps):** The 741 Op Amp, Block diagram, Ideal Op Amp parameters, typical parameter values for 741, equivalent circuit, open loop configurations, voltage transfer curve, frequency response curve.	11
2	**Op Amp with negative feedback:** General concept of Voltage Series, Voltage Shunt, Current Series and Current Shunt negative feedback, Op Amp circuits with Voltage Series and Voltage Shunt feedback, Virtual ground concept. Analysis of inverting and non-inverting amplifier for closed loop gain, Input Resistance and Output Resistance. **Op Amp applications:** Summer, Voltage Follower, Differential and Instrumentation Amplifiers, Integrator, Differentiator, Precision Rectifiers, Comparators, Schmitt Triggers, Log and Antilog amplifiers.	11

3	**Oscillators and Multivibrators:** RC Phase Shift and Wien-bridge Oscillators, Triangular and Sawtooth waveform generators, Astable and Monostable multivibrators. **Active filters:** Comparison with passive filters, First and Second order (Butterworth)Low pass, High pass, Band pass and Band Reject active filters. **Voltage Regulators:** Fixed and Adjustable voltage regulators, IC 723 – Low voltage and High voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.	**11**
4	**Timer and VCO:** Timer IC 555 - Functional diagram, Astable and monostable operations, Basic concepts of Voltage Controlled Oscillator and application of VCO IC LM566. **Phase Locked Loop**: Basic building block, Operation, Lock and capture range, Applications of PLL(Any 4), PLL IC565-block diagram and explanation. **Data Converters:** Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type. Analog to Digital Converters: Specifications, Flash type and Successive approximation type.	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Summarize the concepts of operational amplifiers and differential amplifier configurations	**K2**
CO2	Design operational amplifier circuits for various applications.	**K3**
CO3	Design oscillators and active filters using op-amps.	**K3**
CO4	Outline the working of Timer IC 555, 565 PLL IC, Voltage Regulator ICs and Data converters and various applications using specific integrated circuit chips	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	1	-	2	-	-	-	-	-	1	3	2
CO2	3	2	1	3	2	-	-	-	-	-	2	3	2
CO3	3	2	1		2	-	-	-	-	-	2	3	2
CO4	3	2	1	2	2	-	-	-	-	-	2	3	2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Linear Integrated Circuits	Roy D. C. and S. B. Jain	New Age International	5/e, 2018

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design with Operational Amplifiers and Analog Integrated Circuits	Sergio Franco	Tata McGraw Hill	3/e, 2017
2	Op-Amps and Linear Integrated Circuits	Gayakwad R. A.	Prentice Hall	4/e, 2015
3	Integrated Circuits	Botkar K. R.	Khanna Publishers	10/e, 2013
4	Operational Amplifiers	C.G. Clayton	Butterworth & Company Publ. Ltd. Elsevier	5/e, 2005
5	Operational Amplifiers & Linear Integrated Circuits	R.F. Coughlin & Fredrick Driscoll	PHI	6/e, 2000
6	Operational Amplifiers & Linear ICs	David A. Bell	Oxford University Press	3/e, 2011
7	Microelectronic Circuits	Sedra A. S. and K. C. Smith	Oxford University Press	6/e, 2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117101106
2	https://nptel.ac.in/courses/117101106
3	https://nptel.ac.in/courses/117101106
4	https://nptel.ac.in/courses/117101106

SEMESTER S4
MICROCONTROLLERS

Course Code	**24SJPBECT404**	**CIE Marks**	60
Teaching Hours/Week (L: T:P: R)	3:0:0:1	**ESE Marks**	40
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	24SJPBECT304-Logic Circuit Design	**Course Type**	Theory

Course Objectives:

1. To learn Microcontroller architecture and its programming
2. To learn embedded system design to develop a product.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Microcontroller Architecture – General internal architecture, Address bus, Data bus, control bus. The Microcontroller 8051: Features of 8051 microcontroller, Block diagram of 8051- program status word (PSW), accumulator, program counter. Memory organization – RAM & ROM, register banks and stack, Special Function Registers (SFRs), I/O port organization, Interrupts.	9
2	Instruction Set of 8051 & Addressing modes: Classification of instruction set - Data transfer group, arithmetic group, logical group, branching group. Addressing modes - Types. Accessing the data from internal and external memory. Programming 8051 Using Assembly Language: Introduction to 8051 assembly language programming. Data types & directives, Concept of subroutine. Software delay programming.	9
3	Interfacing with 8051 using Assembly language programming: LED, Seven segment LED display. Programming 8051 Using Embedded C Language- Simple examples – delay generation, Interfacing of – LCD display, Keyboard, Stepper Motor, DAC and ADC -- with 8051 and its programming.	9

4	Timer / Counter in 8051: Timer registers - Timer0, Timer1. Configuration of timer registers. Timer mode programming. Counter mode. Serial Communication in 8051: Serial communication – modes and protocols, RS-232 pin configuration and connection. Serial port programming – transmitting and receiving. Programming the interrupts: Use external, timer and serial port interrupts. Interrupt priority settings	**9**

Suggestion on Project Topics

1. Interface any known ADC chip to 8051 uC. Read the variation in voltage from a potentiometer and display it on an LCD module.
2. Interface any known DAC chip to 8051 uC. Generate a Sine waveform of 1KHz at any port pin.
3. DC motor interface for speed and direction control.
4. Stepper motor interface - Unit step control, Rotation angle control, Speed control, Direction control
5. Read the Temperature sensor and display it on LCD.

Course Assessment Method (CIE: 60 marks, ESE: 40 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Ex-1	Internal Ex-2	Total
5	30	12.5	12.5	60

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 2 marks **(8x2 =16 marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 2 sub divisions. • Each question carries 6 marks. **(4x6 = 24 marks)**	**40**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe the architecture & memory organization of 8051 microcontroller.	**K2**
CO2	Discuss the addressing modes, instruction set and assembly language program of 8051 microcontroller	**K2**
CO3	Explain interrupts, timers and serial communication interface in 8051 and develop programs based on it.	**K3**
CO4	Develop program in assembly or embedded C for interfacing peripheral devices with 8051.	**K3**
CO5	Design and implement an Embedded System	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO 1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	3	-
CO2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO3	3	3	2	-	-	-	-	-	-	-	-	3	-
CO4	3	3	2	-	-	-	-	-	-	-	-	3	-
CO5	3	3	3	3	3	3	3	3	3	3	3	3	3

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The 8051 Microcontroller and Embedded Systems Using Assembly and C	Muhammad Ali Mazidi Janice Gillispie Mazidi Rolin D. McKinlay	Prentice Hall -Inc	Second, 2007
2	The 8051 Microcontroller Architecture, Programming and Applications	Kenneth J Ayala Dhananjay V Gadre	Cengage Learning	2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	8051 hardware Description	Datasheet	Intel Corporation	1992
2	Microprocessors and Microcontrollers	Lyla B. Das	Pearson Education	2011

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	Microprocessors and Microcontrollers - https://nptel.ac.in/courses/106108100
2	Microcontrollers and Applications - https://nptel.ac.in/courses/117104072

PBL Course Elements

L: Lecture (3 Hrs.)	**R: Project (1 Hr.), 1 or 2 Faculty Members**		
	Tutorial	**Practical**	**Presentation**
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation/ Video Presentation: Students present their results in a 2 to 5 minutes video

Assessment and Evaluation for Project Activity

Sl. No	**Evaluation for**	**Allotted Marks**
1	Project Planning and Proposal	10
4	Execution and Implementation	10
5	Final Presentations	10
Total		**30**

1. **Project Planning and Proposal (10 Marks)**

    - Clarity and feasibility of the project plan
    - Research and background understanding
    - Defined objectives and methodology

2. **Execution and Implementation (10 Marks)**

    - Active participation and individual contribution
    - Teamwork and collaboration

    - Adherence to the project timeline and milestones
    - Application of theoretical knowledge and problem-solving
    - Final Result

3. **Final Presentation (10 Marks)**

    - Overall quality and technical excellence of the project
    - Creativity in solutions and approaches

    - Quality and clarity of the overall presentation
    - Individual contribution to the presentation
    - Effectiveness in answering questions

SEMESTER S4

LINEAR INTEGRATED CIRCUITS LAB

Course Code	**24SJPCECL407**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Analog Circuits (24SJPCECT303)	**Course Type**	Lab

Course Objectives:

1. To study the design and implementation of various Linear Integrated Circuits.
2. To familiarize the simulation of basic Linear Integrated Circuits.

Details of Experiment

Expt. No.	**Part A – List of Experiments using Op Amps (Minimum seven experiments mandatory)**
1	Measurement of Op-Amp parameters
2	Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, Integrator, Differentiator - frequency response, Adder, Comparators
3	Difference Amplifier and Instrumentation amplifier
4	Schmitt trigger circuit
5	Astable and Monostable multivibrators
6	Waveform generators using Op Amps - Triangular and Sawtooth
7	Wien bridge oscillator - without & with amplitude stabilization
8	RC Phase shift Oscillator
9	Active first and second order filters (LPF, HPF, BPF and BRF)
10	Active Notch filter to eliminate the 50Hz power line frequency
11	Precision rectifiers
Expt. No	**Part B – Application circuits using ICs [Minimum three experiments are to be done]**
1	Astable and Monostable multivibrator using Timer IC NE555
2	DC power supply using IC 723: Low voltage and high voltage configurations, Short circuit and Fold-back protection.
3	A/D converters- counter ramp and flash type.
4	D/A Converters - R-2R ladder circuit
5	Study of PLL IC: free running, frequency lock range and capture range

Expt No.	**Part C – Simulation experiments** [The experiments shall be conducted using open tools such as QUCS, KiCad or variants of SPICE]]
1	Simulation of any three circuits from experiments 3, 5, 6, 7, 8, 9, 10 and 11 of section I
2	Simulation of experiments 3 or 4 from section II

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- *Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.*
- *Endorsement by External Examiner: The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and implement basic linear integrated circuits using Op Amps.	**K3**
CO2	Design and implement basic linear integrated circuits using linear ICs like 555 timer IC ,565 PLL IC.	**K3**
CO3	Design and simulate the functioning of basic linear integrated circuits and linear ICs. using simulation tools.	**K3**
CO4	Effectively troubleshoot a given circuit and analyze it as a team	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	-	-	-	-	3	-	-	2	3	-
CO2	3	3	2	-	-	-	-	3	-	-	2	3	-
CO3	3	3	2	-	3	-	-	3	-	-	2	3	3
CO4	3	3	2	-	-	-	-	3	-	-	2	3	-

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Linear Integrated Circuits	D. Roy Choudhary and Shail B Jain	New Age International Private Limited	6th edition, 2021
2	Introduction to Pspice Using Orcad for Circuits and Electronics	M. H. Rashid	Pearson	3rd edition, 2015

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Op-Amps And Linear Integrated Circuits: Business Management	Gayakwad	PHI	2002
2	Linear Integrated Circuits	D Roy Choudhury, Shail Bala Jain	New Age International	(2018)

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc24_ee73/preview
2	https://archive.nptel.ac.in/courses/108/108/108108111/

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**
   - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
   - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.
2. **Conduct of Experiments (7 Marks)**
   - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
   - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
   - Teamwork: Collaboration and participation in group experiments.
3. **Lab Reports and Record Keeping (6 Marks)**
   - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
   - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

    - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
    - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
    - Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

    - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

    - Accuracy of Results: Precision and correctness of the obtained results.
    - Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. **Viva Voce (10 Marks)**

    - Ability to explain the experiment, procedure results and answer related questions
    - Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. **Record (5 Marks)**

    - Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S4

MICROCONTROLLER LAB

Course Code	**24SJPCECL408**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	24SJPCECL307- Logic Circuit Design and Simulation Lab	**Course Type**	Lab

Course Objectives:

1. To learn Microcontroller Programming using Assembly and C language
2. To learn Microcontroller interfaces to various modules
3. To learn any advanced microcontrollers like ARM or higher.
4. To learn Embedded System Design

Details of Experiment

Expt. No.	Experiments
	PART A – Data manipulation experiments using Assembly language(Min 4 has to be completed)
1	Multiplication of two 16-bit numbers.
2	Largest/smallest from a series.
3	Sorting (Ascending/Descending) of data.
4	Matrix addition.
5	LCM and HCF of two 8-bit numbers.
6	Code conversion – Hex to Decimal/ASCII to Decimal and vice versa.
7	Find number of odd numbers and number of even numbers present in a given set of numbers
8	Find square of a number and square root of a number
9	Find number of times a given number present in a set of n numbers.
	PART B - Interface to Microcontroller Assembly/C language (Min 3 has to be completed)
1	Time delay generation and relay interface.

2	Display (LED/Seven segments/LCD) and keyboard interface.
3	ADC interface.
4	DAC interface with waveform generation.
5	Stepper motor and DC motor interface.

	PART C - Interface with Advanced Microcontroller using C language (Min 3 has to be completed)
1	PWM generation for DC motor control.
2	Object/Visitor Counter.
3	UART interface to Bluetooth.
4	SPI/I2C interface to display.
5	Real-time clock.

* A minimum of 12 experiments is to be completed.

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	**Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)**	**Internal Examination**	**Total**
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	**Conduct of experiment/ Execution of work/ troubleshooting/ Programming**	**Result with valid inference/ Quality of Output**	**Viva voce**	**Record**	**Total**
10	**15**	**10**	**10**	**5**	**50**

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Develop 8051 Microcontroller programs	**K3**
CO2	Design and implement various interfaces to the 8051 Microcontroller	**K3**
CO3	Design and implement an Embedded System using an advanced microcontroller	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	2	3	-	-	-	-	-	2	3	3
CO2	3	3	2	2	3	-	-	-	-	-	2	3	3
CO4	3	3	2	2	3	3	3	3	3	-	3	3	3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The 8051 Microcontroller and Embedded Systems Using Assembly and C	Muhammad Ali Mazidi Janice Gillispie Mazidi Rolin D. McKinlay	Printice Hall -Inc	Second, 2007
2	The 8051 Microcontroller Architecture, Programming and Applications	Kenneth J Ayala Dhananjay V Gadre	Cengage Learning	2010

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	8051 Hardware Description	Datasheet	Intel Corporation	1992
2	Microprocessors and Microcontrollers	Lyla B. Das	Pearson Education	2011
3	ARM System-on-Chip Architecture	Steve Furber	Addison-Wesley Educational Publishers Inc	2000
4	System-on-Chip Design with Arm(R) Cortex(R)-M Processors	Joseph Yiu	ARM Education Media	2019

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	Microprocessors and Microcontrollers - https://nptel.ac.in/courses/106108100
2	Microcontrollers and Applications - https://nptel.ac.in/courses/117104072
3	Embedded System Design With ARM - https://onlinecourses.nptel.ac.in/noc22_cs93

Continuous Assessment (25 Marks)

1. **Preparation and Pre-Lab Work (7 Marks)**
   - Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
   - Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.
2. **Conduct of Experiments (7 Marks)**
   - Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
   - Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
   - Teamwork: Collaboration and participation in group experiments.
3. **Lab Reports and Record Keeping (6 Marks)**
   - Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
   - Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**
    - Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**
    - Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
    - Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
    - Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
    - Creativity and logic in algorithm or experimental design.
2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**
    - Setup and Execution: Proper setup and accurate execution of the experiment or programming task.
3. **Result with Valid Inference/Quality of Output (10 Marks)**
    - Accuracy of Results: Precision and correctness of the obtained results.
    - Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.
4. **Viva Voce (10 Marks)**
    - Ability to explain the experiment, procedure results and answer related questions
    - Proficiency in answering questions related to theoretical and practical aspects of the subject.
5. **Record (5 Marks)**

    Completeness, clarity, and accuracy of the lab record

COURSES - PROGRAM ELECTIVE – 1

PROGRAM ELECTIVE I: 24SJPEECT41N					
SLOT	**COURSE CODE**	**COURSES**	**L-T-P-R**	**HOURS**	**CREDIT**
E	**24SJPEECT411**	Instrumentation	3-0-0-0	**3**	3
	24SJPEECT412	Power Electronics	3-0-0-0		3
	24SJPEECT413	Machine Learning	3-0-0-0		3
	24SJPEECT414	Object Oriented Programming	3-0-0-0		3
	24SJPEECT416	Digital System Design	3-0-0-0		3
	24SJPEECT415	Digital Systems and VLSI Design	3-0-0-0		**5/3**

Note : Level 5 courses in the B. Tech curriculum carry a total of 5 credits, consisting of 3 credits for the Programme Elective and 2 additional credits. The additional 2 credits shall be awarded only if the student meets the eligibility conditions specified in the B. Tech. -2024 regulations. If those conditions are not fulfilled, the student will receive only 3 credits for the course.

SEMESTER S4

INSTRUMENTATION

Course Code	**24SJPEECT411**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None/ (Course code)	**Course Type**	Theory

Course Objectives:

1. This course aims to introduce the basic concepts of electronic measuring instruments.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to measuring instruments** Generalized Configurations and Functional elements of Instrumentation systems, Need for Measurement Systems, Classification of Types of Measuring instruments. Static and Dynamic characteristics of measuring instruments.	9
2	**Sensors and Transducers** Classification and selection criteria of Transducers Principles of operation, construction, theory, advantages and disadvantages , applications of **Resistive Transducers:** Potentiometers, strain gauges, (metallic and semi-conductor type), Resistance Thermometer, Thermistors. **Inductive Transducers:** LVDT (Linear variable differential transformer). **Capacitive Transducers:** various capacitive transducers based upon familiar equation of capacitance (capacitive microphone)	9

3	**Electronic Measuring Instruments** Digital storage oscilloscope, Working principle and applications of waveform analyser, digital frequency meter, harmonic distortion meter, harmonic analyser, spectrum analyser and logic state analyser IEEE -488 General Purpose Interface Bus (GPIB) Instruments with application. EMI,Grounding and Shielding	**9**
4	**PLC Programming** Basic PLC Programming: Programming ON/OFF Inputs, Creating Ladder diagrams, Register Basics, PLC Timers and Counters, PLC Arithmetic functions, Number comparison functions, Data handling Functions: Skip function and applications; master control relay function and applications; jump with non-return and return; data table, register nd other move functions, PLC functions with BITS.	**9**

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	**Assignment/ Micro project**	**Internal Examination- 1 (Written)**	**Internal Examination- 2 (Written)**	**Total**
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	**Part B**	**Total**
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Interpret the basic concepts of measuring instruments, its classification, and selection criteria.	**K2**
CO2	Outline the principle, construction and working of transducers for measuring physical variables.	**K2**
CO3	Comprehend the principle, construction and working of various electronic measuring instruments.	**K2**
CO4	Apply PLC programming for selected industrial processes.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	-	-	1	-	-	-	-	-	2	1	-
CO2	3	3	2	-	1	-	-	-	-	-	2	1	-
CO3	3	3	2	-	2	-	-	-	-	-	2	-	-
CO4	3	3	3	-	3	-	-	2	-	-	2	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Doebelin's Measurement Systems	Ernest Doebelin, Dhanesh N. Manik	Tata McGraw Hill	6/e, 2011
2	Electronic Instrumentation	Kalsi H S	Tata McGraw Hill	4/e, 2019
3	Programmable Logic controllers Programming Methods and Applications	John R Hackworth, Frederick D Hackworth	Pearson Education	3/e, 2022

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	"Electrical and Electronics Measurements and Instrumentation,"	Sawhney AK,	Dhanpat Rai and Sons	2023
2	"Programmable Logic Controllers- Principles and applications	John W Webb, Ronald A. Reis,	Pearson	5/e, 2015

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/108/105/108105064/
2	https://archive.nptel.ac.in/courses/108/105/108105153/

SEMESTER S4

POWER ELECTRONICS

Course Code	**24SJPEECT 412**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Analog Circuits (PCECT303**)**	**Course Type**	Theory

Course Objectives:

1. To study the characteristics of power electronic devices.
2. To study different power converter circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction:** Scope and applications of Power Electronics, Properties of ideal switch. **Structure and static characteristics:** Power diodes, Power BJT, Power MOSFET & IGBT – comparison. Basic principles of wide band gap devices – SiC & GaN. **Safe Operating Area:** Power BJT, Power MOSFET & IGBT. **Drive Circuits:** Power BJT and Power MOSFET (any two example circuits – no analysis).	**9**
2	**SCR:** Structure, two transistor analogy, static characteristics. **Rectifiers:** Three phase diode bridge rectifiers, Single phase half-controlled rectifier with R load – Single phase fully controlled bridge rectifier (continuous conduction) – output voltage equation. Principle of three phase half wave controlled rectifier– (average output voltage equation for continuous load current) – related simple problems (1-phase & 3-phase).	**9**
3	**DC – DC Switch Mode Converters:** Buck, Boost and Buck-boost DC-DC converters. Waveforms and expression of DC-DC converters for output voltage, voltage and current ripple under continuous conduction mode.	**9**

	Isolated converters: Flyback, Forward, Push Pull, Half bridge and Full bridge converters – Waveforms and governing equations.	
4	**DC-AC Switch Mode Inverters:** Inverter topologies, Driven Inverters: Push-Pull, Half bridge and Full bridge configurations, Single phase PWM inverters (Single pulse width and sinusoidal pulse width modulation) – rms output voltage equation and output voltage waveforms.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Outline the working and key characteristics of power semiconductor devices such as Power Diode, BJT, MOSFET, and IGBT.	**K2**
CO2	Describe the working of SCR and rectifier circuits and find the output voltage for different types of rectifiers.	**K3**
CO3	Apply the working of DC-DC converters to find output voltage and ripple for different converter types.	**K3**
CO4	Apply inverter topologies and PWM methods to analyze the output voltage and waveform of DC-AC converters.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	1	1	-
CO2	3	-	2	-	1	-	-	-	-	-	1	1	-
CO3	3	2	2	3	2	-	-	-	-	-	1	1	-
CO4	3	1	3	3	2	1	-	-	-	-	-	1	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Power Electronics Essentials & Applications	L Umanand	Wiley India	Reprint Edition 2014
2	Power Electronics Circuits, Devices, and Applications	Muhammad H Rashid	Pearson India	Third Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Power Electronics Converters, Applications, and Design	Ned Mohan, Tore M Undeland, William P. Robbins	Wiley India	Third Edition
2	Power Electronics Principles and Applications	Joseph Vithayathil	Tata McGraw-HILL	Second Reprint 2010
3	Power Electronics	Daniel W Hart	McGraw-HILL	2011
4	SiC and GaN Wide Bandgap Device Technology Overview,	Milligan, J. W., Sheppard, S., Pribble, W., Wu, Y.-F., Muller, G., &Palmour, J. W	2007 IEEE Radar Conference.	doi:10.1109/radar.2007.374395.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://www.youtube.com/watch?v=fOZ8bUrFJGk
2	https://archive.nptel.ac.in/courses/117/108/117108124/
3	https://www.youtube.com/watch?v=Dg5AIy0bY1A

SEMESTER S4

MACHINE LEARNING

Course Code	24SJPEECT413	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	NONE	**Course Type**	Theory

Course Objectives:

1. To provide a comprehensive understanding of machine learning principles and techniques.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Review**: supervised, unsupervised machine learning techniques, dimensionality reduction techniques-PCA, SVD. Instance-Based vs Model-Based Learning, Machine Learning models, Hyper parameters, regularization, Training - Batch and Online Learning, **Challenges of Machine Learning**: Data Issues-Quality, Relevancy, Over fitting, under fitting. Bias, variance, **Performance metrics:** Accuracy,Recall, Precision, ROC curve	9
2	**Regression**: linear regression, logistic regression error functions in regression, MSE, L1, L2, Cross entropy multivariate regression. **Classification**: Naive Bayes classifier, Support Vector machines, Decision trees -random forests, Ensemble methods: boosting, bagging.	9
3	**Unsupervised learning**: Clustering-K-means, High, Hierarchical clustering, criterion functions for clustering, proximity measures, Euclidean, Manhattan, Minkowski Distances, Cosine Similarity. **Reinforcement Learning**: Agent based learning, Q-learning, Introduction to HMM models	7

4	**Introduction to Artificial Neural Networks**: Biological Neuron, Perceptron, Training, limitations, XOR problem, Multilayer perceptron, Gradient based learning, stochastic gradient descent, Activation Functions-Sigmoid, ReLU, tanh. Back propagation- Chain rule, Regularization- L1, L2,	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply supervised and unsupervised machine learning techniques to solve various data-driven problems.	K3
CO2	Develop, train, and optimize regression and classification models	K3
CO3	Design and execute clustering techniques, and assess their effectiveness using various proximity measures.	K3
CO4	Apply unsupervised learning techniques and understand reinforcement learning for complex problem-solving.	K3

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	-	1	-	-	-	-	-	2	1	-
CO2	3	2	2	-	1	-	-	-	-	-	2	-	-
CO3	3	2	2	-	1	-	-	-	-	-	2	-	-
CO4	3	2	2	-	1	-	-	-	-	-	2	-	-

Note: 1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Hands-on Machine learning with Sc-kit Learn Keras and Tensorflow (module 1)	Aurelien Geron	Oreilly	Second edition 2019
2	Machine learning for absolute beginners	Oliver Theobald		Second edition
3	Learning Deep Learning (for module 4)	Magnus Ekman	Addison -Wesley	2022
4	Introduction to Machine learning with Python	Andreas C. Müller & Sarah Guido	O'Reilly	2017

Reference Books

Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	"Pattern Recognition and Machine Learning"	. Bishop, C. M.	Springer, New York,	2006.
2	"Pattern Recognition".	Theodoridis, S. and Koutroumbas, K.	Academic Press, San Diego,.	2003
3	Artificial Intelligence : a Modern Approach.	Russell, Stuart J.	Prentice Hall,	2010.
4	CS229 Lecture Notes	Andrew Ng and Tengyu Ma	https://cs229.stanford.edu/main_notes.pdf	2023

Video Links (NPTEL, SWAYAM…)	
Module No.	Link ID
1	https://onlinecourses.nptel.ac.in/noc23_cs18/preview (For modules 1,2 and 3)
2	https://see.stanford.edu/Course/CS229
3	https://onlinecourses.nptel.ac.in/noc23_cs18/preview
4	https://www.3blue1brown.com/topics/neural-networks

SEMESTER S4

OBJECT ORIENTED PROGRAMMING

Course Code	**24SJPEECT414**	**CIE Marks**	**40**
Teaching Hours/Week (L: T:P: R)	**3:0:0:0**	**ESE Marks**	**60**
Credits	**3**	**Exam Hours**	**2 Hrs. 30 Min.**
Prerequisites (if any)	**PROGRAMMING IN C**	**Course Type**	**Theory**

Course Objectives:

1. To introduce the basic concepts of object-oriented design techniques.
2. To give a thorough understanding of the basics of Java programming

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction: Approaches to Software Design - Functional Oriented Design, Object Oriented Design, Case Study of Automated Fire Alarm System. Introduction to Java - Java Buzzwords, Java program structure, Java compiler, Bytecode, Java Virtual Machine (JVM), Comments, Lexical Issues.	7
2	Core Java Fundamentals: Primitive Data types - Integers, Floating Point Types, Characters, Boolean. Literals, Variables, Type Conversion and Casting, Arrays, Strings- String Handling functions. Operators - Arithmetic Operators, Bitwise Operators, Relational Operators, Boolean Logical Operators, Assignment Operator, Conditional (Ternary) Operator, Operator Precedence. Control Statements - Selection Statements, Iteration Statements and	9

	Jump Statements. **Object Oriented Programming in Java** - Class Fundamentals, Declaring Objects, Object Reference, Access Control, Introduction to Methods, Constructors, this Keyword, Method Overloading. Inheritance - Super Class, Sub Class, The Keyword super, protected Members, Method Overriding.	
3	More features of Java: Packages - Defining Package, CLASSPATH, Importing Packages. Exception Handling - Checked Exceptions, Unchecked Exceptions, try Block and catch Clause, Multiple catch Clauses, Nested try Statements, throw, throws and finally. Input/output - I/O Basics, Reading Console Input, Writing Console Output, Print Writer Class, Working with Files.	10
4	Advanced features of Java: Swings fundamentals - Swing Key Features, Model View Controller (MVC), Swing Controls, Components and Containers, Swing Packages, Event Handling in Swings, Swing Layout Managers, Exploring Swings –JFrame, JLabel, The Swing Buttons, JtextField.. Java DataBase Connectivity (JDBC) - JDBC overview, Creating and Executing Queries – create table, delete, insert, select.	10

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks (8x3 =24marks)	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. (4x9 = 36 marks)	60

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Summarize the object-oriented concepts - classes, objects, constructors, data hiding, inheritance and polymorphism and to illustrate it using UML diagrams.	K2
CO2	Utilise datatypes, operators, control statements, object oriented class, object concepts in Java to develop programs.	K3
CO3	Illustrate how robust programs can be written in Java using packages, exception handling mechanism and Input/ Output Streams with Files.	K3
CO4	Identify and utilize various Swing controls, components, and containers.	K3

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	-	-	-	-	-	-	-	3	3	-
CO2	3	2	2	-	-	-	-	-	-	-	3	3	-
CO3	3	2	2	-	-	-	-	-	-	-	3	3	-
CO4	3	2	2	-	-	-	-	-	-	-	3	3	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Java: The Complete Reference	Herbert Schildt	Tata McGraw Hill	8/e, 2011.
2	Fundamentals of Software Engineering,	Rajib Mall	PHI	4th edition, 2014.
3	Java How to Program, Early Objects	Paul Deitel, Harvey Deitel,	Pearson,	11th Edition, 2018.

Reference Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Programming JAVA a Primer	Balagurusamy E	McGraw Hill	5/e, 2014.
2	Object Oriented Systems Development using the Unified Modeling Language	Ali Bahrami	McGraw-Hill Int.	2017
3	Introduction to Java Programming	Y. Daniel Liang	Pearson	7/e, 2013.
4	Core Java: An Integrated Approach	Nageswararao R.	Dreamtech Press	2008
5	Java in A Nutshell	Flanagan D	O'Reilly	5/e, 2005.
6	Object Oriented Design with UML and Java	Barclay K.J. Savage,	Elsevier	2004
7	Head First Java	Sierra K.	O'Reilly	2/e, 2005.

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	**https://onlinecourses.nptel.ac.in/noc20_cs08/preview**

SEMESTER S4

DIGITAL SYSTEM DESIGN

Course Code	**24SJPEECT416**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	**24SJPBECT304**: Logic Circuit Design	**Course Type**	Theory

Course Objectives:

1. To acquire knowledge about Asynchronous and clocked Synchronous sequential circuit design.
2. To detect the faults and hazards in digital circuit design
3. To design and implement digital circuits using VHDL.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Finite state machines - Mealy and Moore models, State graphs, State assignment, State table, State reduction. Clocked Synchronous Networks, Analysis of Clocked Synchronous Sequential Networks (CSSN), Modeling of CSSN, State assignment and reduction, Design of CSSN.	**12**
2	ASM Chart and its realization. Asynchronous Sequential Circuits, Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction, Races in ASC, State assignment problem and the transition table.	**10**
3	Hazards – static and dynamic hazards in combinational networks, Essential Hazards, Design of Hazard free circuits, Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs. Faults: Fault table method – path sensitization method – Boolean difference method.	**8**

4	VLSI Design flow: Design entry: Schematic, Data types and objects, different modelling styles in Verilog/VHDL - Dataflow, Behavioural and Structural Modelling. Verilog constructs and codes for combinational and sequential circuits.	**8**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Micro project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design asynchronous and clocked synchronous sequential circuits	**K3**
CO2	Design and realize asynchronous sequential circuits	**K3**
CO3	Understand basic concepts fault-free in digital circuits	**K2**
CO4	Apply VHDL/Verilog programming in digital system design	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	3	3	-	-	-	2	-	1	3	1	-
CO2	3	2	2	2	-	-	-	2	-	1	3	1	-
CO3	3	3	2	-	-	-	-	2	-	1	3	-	-
CO4	3	3	3	3	3	-	-	2	-	-	3	2	2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Principles & Design	Donald G Givone	Tata McGraw Hill	1/e 2002
2	Digital Design with an introduction to HDL, VHDL and Verilog	M.Morris Mano and Michel.D.Ciletti	Pearson education	6/e, 2018
3	Digital Design	John F Wakerly	Pearson Education	4/e 2008
4	Digital Logic Applications and Design	John M Yarbrough	Cengage India	1/e 2006

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Systems Testing and Testable Design	Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman	John Wiley & Sons Inc	1994
2	Logic Design Theory	N. N. Biswas	PHI	1992
3	Introduction to Digital Design Using Digilent FPGA Boards	Richard E. Haskell, Darrin M. Hanna	LBE Books- LLC	2009
4	Digital Circuits and Logic Design	Samuel C. Lee	PHI	1980
5	Digital System Design Using VHDL	R. Anand	Khanna Book Publishing Company	FIRST,201 3
6	Digital System Design using VHDL	Charles Roth	PWS PUBLISHING	1997
7	Digital System Design Using VHDL	Lizy Kurian John, Charles H. Roth	Cengage	1ST 2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/
3	https://archive.nptel.ac.in/courses/108/105/108105132/ Lecture 15
4	https://nptel.ac.in/courses/108106177

SEMESTER S4

DIGITAL SYSTEMS AND VLSI DESIGN

Course Code	**24SJPEECT415**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	**ESE Marks**	60
Credits	5/3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	24SJPBECT304 Logic Circuit Design	**Course Type**	Theory

Course Objectives:

1. To equip students with comprehensive knowledge and skills in designing, analysing, modelling, and optimizing clocked synchronous sequential networks (CSSNs).
2. To provide a thorough understanding of the designing, analyzing, and optimizing techniques of asynchronous sequential circuits (ASCs).
3. To equip students with the knowledge and skills to identify and mitigate static and dynamic hazards and to understand fault detection and testing methods.
4. To provide students with a comprehensive understanding of the VLSI design flow and the application of HDL coding for combinational and sequential circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Clocked Synchronous Networks, Analysis of Clocked Synchronous Sequential Networks (CSSN), Mealy machine, Moore machine, Modelling of CSSN, State assignment and reduction, Design of CSSN, ASM Chart and its realization.	**9**
2	Asynchronous Sequential Circuits, Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction, Races in ASC, State assignment problem and the transition table, Design of Asynchronous Sequential Circuits, Design of ALU.	**9**

3	Hazards – static and dynamic hazards in combinational networks, Essential Hazards, Design of Hazard free circuits, Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs, Flip-Flops and Simple Flip-Flop Applications, switch debouncer. Faults, Fault table method – path sensitization method – Boolean difference method, Kohavi algorithm, Automatic test pattern generation – Built in Self-Test (BIST)	**9**
4	VLSI Design flow: Design entry: Schematic, FSM & HDL, VHDL/Verilog Hardware Description Language, Modules, Data types and operators, Objects, Different modeling styles- Dataflow, Behavioral and Structural Modeling, Synthesis, Simulation. VHDL/Verilog codes for combinational and sequential circuits.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	*Internal Ex*	*Evaluate*	*Analyse*	*Total*
5	**15**	**10**	**10**	**40**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

Evaluation Methods:

1. Experiments Using Design and Analysis Tools: (10 marks)

Students can perform specific experiments using tools like GHDL, iVerilog, ModelSim, Xilinx ISE, Vivado etc.

Each experiment can focus on designing and simulating different types of circuits (synchronous, asynchronous, combinational, sequential).

2. Course Project:

Comprehensive project involving design, modeling, and analysis of a digital system. (10 marks)

Project phases: Proposal, Design, Implementation, Testing, Final Report.

Presentations and Viva Voce:

Students present their projects and experiments, explaining design choices, methodologies, and results.

Viva voce to assess understanding and ability to answer related questions.

Sample Experiments:

Experiment 1: Basic Mealy/Moore Machine Design

- **Objective:** Design a simple Mealy/Moore machine to detect a specific sequence of bits (e.g., "101").
- **Tools:** VHDL/Verilog, GHDL, iVerilog, ModelSim/Xilinx ISE, Vivado.
- **Steps:**
    1. Draw the state diagram for the sequence detector.
    2. Write the VHDL or Verilog code for the Mealy machine.
    3. Simulate the design to verify its functionality.

Experiment 2: Basic Flow Table Reduction

- **Objective:** Reduce the flow table for a simple asynchronous sequential circuit.
- **Tools:** Manual calculation, VHDL/Verilog for verification.
- **Steps:**
    1. Given a flow table, perform flow table reduction.
    2. Assign binary codes to the reduced states.
    3. Implement the reduced state machine in VHDL or Verilog and simulate it.

Experiment 3: Identifying and Eliminating Static Hazards

- **Objective:** Identify and eliminate static hazards in a simple combinational circuit.
- **Tools:** VHDL/Verilog, GHDL, iVerilog, ModelSim/Xilinx ISE, Vivado.
- **Steps:**
    1. Design a combinational circuit with a known static hazard.
    2. Identify the static hazard in the circuit.
    3. Modify the design to eliminate the static hazard and simulate it.

Experiment 4: Fault Detection Using Path Sensitization

- **Objective:** Use the path sensitization method to detect faults in a simple digital circuit.
- **Tools:** VHDL/Verilog, GHDL, iVerilog, ModelSim/Xilinx ISE, Vivado.
- **Steps:**

1. Design a simple digital circuit.
2. Apply the path sensitization method to detect faults.
3. Implement and simulate the circuit in VHDL or Verilog to verify fault detection.

Sample Project Topics:

1. Design and Analysis of a Traffic Light Controller Using Mealy and Moore Machines
2. State Reduction and Assignment for a Sequence Detector
3. Design and Analysis of an Asynchronous Sequence Detector
4. Designing a Simple Arithmetic Logic Unit (ALU) with Flow Table Reduction and Hazard Handling
5. Design of a Hazard-Free Circuit for a Critical Application
6. Implementing Data Synchronizers for Mixed Operating Mode Asynchronous Circuits
7. Comprehensive VLSI Design Project Using VHDL (e.g., Digital Clock, ALU, Traffic Light Controller)
8. Synthesis and Simulation of Complex Sequential Circuits Using Different VHDL Modeling Styles

Criteria for Evaluation: Lab Experiments (10 marks)

1. **Understanding of Concepts (3 marks)**
   - Demonstrates a clear understanding of the theoretical concepts related to the experiment.
   - Correctly explains the purpose and expected outcomes of the experiment.
2. **Implementation and Accuracy (3 marks)**
   - Correctly implements the design using appropriate tools.
   - The design functions as expected without errors.
3. **Analysis and Problem-Solving (2 marks)**
   - Effectively analyse the design to identify and resolve issues.
   - Demonstrates problem-solving skills in addressing any encountered challenges.
4. **Documentation and Reporting (1 mark)**
   - Provides clear and concise documentation of the steps and processes followed.
   - The report includes diagrams, code snippets, and simulation results.

5. **Presentation and Communication (1 mark)**
    - Clearly presents the experiment and its results.
    - Able to answer questions and explain the design choices.

Criteria for Evaluation: Course Project (10 marks)

1. **Project Proposal and Planning (10 marks)**
    - Submits a well-defined project proposal outlining objectives, methodology, and expected outcomes.
    - Demonstrates thorough planning and a clear timeline for the project.
2. **Design and Implementation (10 marks)**
    - Implements the project design accurately using appropriate tools and techniques.
    - The design is functional and meets the project objectives.
3. **Final Report and Presentation (10 mark)**
    - Submits a comprehensive final report detailing the project, including objectives, design, methodology, analysis, and results.
    - Clearly presents the project and its outcomes, and effectively communicates the key points.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. • Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design, analyze, and model clocked synchronous sequential networks (CSSNs), optimize state assignment and reduction, and effectively utilize ASM charts for the realization of complex digital systems.	**K3**
CO2	Design and analyze asynchronous sequential circuits (ASCs), perform flow table reduction, address race conditions and state assignment problems, and design both ASCs and Arithmetic Logic Units (ALUs).	**K3**
CO3	Identify and mitigate static and dynamic hazards in combinational networks, design hazard-free circuits, address practical issues in digital systems and apply fault detection and testing methods.	**K3**
CO4	Explain the VLSI design flow, utilize various design entry methods, apply different VHDL/Verilog modeling styles, and develop and simulate VHDL/Verilog codes for combinational and sequential circuits.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	-	-	-	-	-	-	-	-	1	-
CO2	3	2	2	-	-	-	-	-	-	-	-	1	-
CO3	3	1	2	-	-	-	-	-	-	-	-	-	-
CO4	1	1	2	2	2	-	-	-	-	-	-	-	-

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Principles & Design	Donald G Givone	McGraw Hill Education	2017
2	Digital Design: Principles and Practices	John F Wakerly	Pearson India	4th, 2008
3	Digital Logic Applications and Design	John M Yarbrough	Cengage Learning India	1st, 2006
4	Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog	M.Morris Mano and Michel.D.Ciletti,	Pearson	6th, 2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Systems Testing and Testable Design	Melvin A. Breuer, Miron Abramovici, Arthur D. Friedman	Wiley-IEEE Press	1st, 1994
2	Logic Design Theory	Nripendra N. Biswas	Prentice Hall	1993
3	Introduction to Digital Design Using Digilent FPGA Boards: Block Diagram / VHDL Examples	Richard E. Haskell Darrin M. Hanna	LBE Books- LLC	2019
4	Digital Circuits and Logic Design	Samuel C. Lee	Prentice Hall India Learning Private Limited	1980
5	Switching and Finite Automata Theory	Zvi Kohavi, Niraj K. Jha	CAMBRIDGE UNIVERSITY PRESS	3rd 2009
6	Digital System Design Using VHDL	Rishabh Anand	Khanna Publishing	1st, 2013
7	Digital System Design Using VHDL	Lizy Kurian John, Charles H. Roth	Cengage	1st, 2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/
3	https://archive.nptel.ac.in/courses/108/105/108105132/ (Lecture 15)
4	https://nptel.ac.in/courses/108106177

Programme Outcomes (POs)

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyse complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyse and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10:Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

Knowledge and Attitude Profile (WK)

WK1: A systematic, theory-based understanding of the natural sciences applicable to the discipline and awareness of relevant social sciences.

WK2: Conceptually-based mathematics, numerical analysis, data analysis, statistics and formal aspects of computer and information science to support detailed analysis and modelling applicable to the discipline.

WK3: A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline.

WK4: Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline.

WK5: Knowledge, including efficient resource use, environmental impacts, whole-life cost, re-use of resources, net zero carbon, and similar concepts, that supports engineering design and operations in a practice area.

WK6: Knowledge of engineering practice (technology) in the practice areas in the engineering discipline.

WK7: Knowledge of the role of engineering in society and identified issues in engineering practice in the discipline, such as the professional responsibility of an engineer to public safety and sustainable development.

WK8: Engagement with selected knowledge in the current research literature of the discipline, awareness of the power of critical thinking and creative approaches to evaluate emerging issues.

WK9: Ethics, inclusive behaviour and conduct. Knowledge of professional ethics, responsibilities, and norms of engineering practice. Awareness of the need for diversity by reason of ethnicity, gender, age, physical ability etc. with mutual understanding and respect, and of inclusive attitudes.

Department of

Electronics and Communication Engineering

Vision

Develop into a center of excellence in Electronics and Communication Engineering contributing to socio-economic progress.

Mission

- To develop and maintain adequate infrastructure for a pace-setting Electronics and Communication engineering.
- To bring up a team of committed, proficient and research-oriented electronics and communication engineering faculty.
- To nurture students into ethical, emotionally strong and technically competent graduates to meet the dynamic challenges of the society.