ST. JOSEPH'S
COLLEGE OF ENGINEERING
AND TECHNOLOGY,
- PALAI -
AUTONOMOUS

Choondacherry P.O., Pala, Kottayam-686579
Kerala, India

CURRICULUM & SYLLABUS

B. Tech (Honours) *in*
ELECTRONICS AND COMMUNICATION ENGINEERING

2024 SCHEME

www.sjcetpalai.ac.in

Signed By: Devassia V P
Reason: Approved by SJCET Academic Council held on 25.11.2025

CURRICULUM

B.Tech (Honours) is an enhanced version of the Bachelor of Technology degree, offering the students the opportunity to undertake additional courses within their own discipline. This pathway allows students to deepen their knowledge in emerging or advanced areas of Engineering relevant to their field of study, providing a stronger foundation for specialized career paths or further academic pursuits.

For the award of B.Tech (Honours) in Electronics and Communication Engineering, the student shall fulfil all the curricular requirements for B.Tech in Electronics and Communication Engineering as per SJCET B.Tech Academic Regulations 2024 and shall earn 15 additional credits by undergoing the following courses, which shall be further governed by clause R16 of the Regulations.

Sl. No	Semester	Course Code	Course Name/Type	Weekly hours				Total Marks		Credits
				L	T	P	SS	CIE	ESE	
1	4	24SJHNECT401	NANO ELECTRONICS	3	1	0	5	40	60	4
2	5	24SJHNECT501	FPGA BASED SYSTEM DESIGN	3	1	0	5	40	60	4
		24SJHNECM5XX	Approved MOOC *							
3	6	24SJHNECT601	ELECTRONIC DESIGN AUTOMATION	3	1	0	5	40	60	4
		24SJHNECM6XX	Approved MOOC *							
4	7	24SJHNECT701	RF MEMS	3	0	0	5	40	60	3
		24SJHNECM7XX	Approved MOOC *							
Total Credits										15

*MOOC to be approved by the Academic Council on recommendation of the Board of Studies.

SEMESTER 4

24SJHNECT401	NANOELECTRONICS	CATEGORY	L	T	P	CREDIT
		Honours	3	1	0	4

Preamble: This course aims to understand the physics behind mesoscopic systems and working of nanoelectronic devices.

Prerequisite: 24SJPCECT302 Solid State Devices

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain quantum mechanical effects associated with low dimensional semiconductors.	K2
CO 2	Explain the different processes involved in the fabrication of nanoparticles and nanolayers.	K2
CO 3	Explain the different techniques for characterizing nano layers and particles	K2
CO 4	Explain the different transport mechanisms in nanoscale structures and illustrate the operating principles of nanoscale electronic devices, such as SET, Resonant tunnelling devices, and Quantum lasers.	K2

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PSO 1	PSO2
CO1	2	-	-	1	-	-	-	-	-	-	-	2	-
CO2	2	-	-	-	-	-	-	-	-	-	-	2	-
CO3	1	-	-	-	2	-	-	-	-	-	-	2	-
CO4	2	-	-	1	2	-	-	-	-	-	-	2	-

Syllabus

Module I

Introduction to nanotechnology, Limitations of conventional microelectronics, characteristic lengths in mesoscopic systems, Quantum mechanical coherence.

Low dimensional structures - Quantum wells, wires and dots, Density of states of 1D and 2D nanostructures.

Basic properties of square quantum wells of finite depth, parabolic and triangular quantum wells

Module II

Introduction to methods of fabrication of nano-layers: physical vapour deposition- evaporation & Sputtering, Chemical vapour deposition, Molecular Beam Epitaxy, Ion Implantation, Formation of Silicon Dioxide- dry and wet oxidation methods.

Fabrication of nano particle- grinding with iron balls, laser ablation, reduction methods, sol gel, self assembly, precipitation of quantum dots.

Module III

Introduction to characterization of nanostructures: Principle of operation of Scanning Tunnelling Microscope, Atomic Force Microscope, Scanning Electron microscope - specimen interaction, X- Ray Diffraction analysis

Module IV

Quantum wells, multiple quantum wells, Modulation doped quantum wells, concept of super lattices Kronig - Penney model of super lattice.

Transport of charge in Nanostructures - Electron scattering mechanisms, Hot electrons, Resonant tunnelling transport, Coulomb blockade, Effect of magnetic field on a crystal. Aharonov-Bohm effect, the Shubnikov-de Hass effect.

Nanoelectonic devices - MODFETS, Single Electron Transistor, CNT transistors – Properties of graphene, Resonant tunnel effect, RTD, RTT, Hot electron transistors Quantum well laser, quantum dot LED, quantum dot laser

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Text Books

1. J.M. Martinez-Duart, R.J. Martin Palma, F. Agulle Rueda Nanotechnology for Microelectronics and optoelectronics , Elsevier, 2006

2. W.R. Fahrner, Nanotechnology and Nanoelctronics, Springer, 2005

Reference Books

1. Chattopadhyay, Banerjee, Introduction to Nanoscience & Technology, PHI 2012
2. Poole, Introduction to Nanotechnology, John Wiley 2006.
3. George W. Hanson, Fundamentals of Nanoelectronics, Pearson Education, 2009.
4. K. Goser, P. Glosekotter, J. Dienstuhl, Nanoelectronics and nanosystems, Springer 2004.
5. Supriyo Dutta, Quantum Transport- Atom to transistor, Cambridge, 2013.

SEMESTER 5

24SJHNECT501	FPGA BASED SYSTEM DESIGN	CATEGORY	L	T	P	CREDIT
		Honours	3	1	0	4

Preamble: This course aims to develop the skill of FPGA based system design.

Prerequisite: 24SJPCECT304 Logic Circuit Design

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply VLSI design methodology and state machine design concepts to design and implement simple digital systems using hardware description languages.	K3
CO 2	Apply knowledge of Programmable Logic Devices to design and implement MSI circuits using appropriate PLD-based techniques.	K3
CO 3	Understand FPGA architecture and the design considerations of FPGA.	K2
CO4	Discuss commercial FPGAs and design simple combinational and sequential circuits using FPGA	K3

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PSO 1	PSO2
CO 1	3	3	-	-	2	-	-	-	-	-	2	2	2
CO 2	3	3	-	-	2	-	-	-	-	-	2	2	2
CO 3	3	3	-	-	2	-	-	-	-	-	2	2	2
CO 4	3	3	-	-	2	-	-	-	-	-	2	2	2

SYLLABUS

Module 1:

Introduction: Digital system design options and tradeoffs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modelling and simulation, Hardware description languages (emphasis on Verilog), combinational and sequential design, state machine design, synthesis issues, test benches.

Module 2:

Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Limitations, Architectures and Programming. Implementation of MSI circuits using Programmable logic Devices.

Module 3:

FPGA architecture: FPGA Architectural options, granularity of function and wiring resources, coarse V/s fine grained, vendor specific issues (emphasis on Xilinx and Altera), Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation.

Module 4:

Placement and Routing: Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications -Embedded system design using FPGAs, DSP using FPGAs.

Commercial FPGAs: Xilinx, Altera, Actel (Different series description only), Case study Xilinx Virtex: implementation of simple combinational and sequential circuits.

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Text Books

1. FPGA-Based System Design Wayne Wolf, Verlag: Prentice Hall
2. Modern VLSI Design: System-on-Chip Design (3rd Edition) Wayne Wolf, Verlag

Reference Books

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic
2. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall
3. Field programmable gate array, S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, 2007, BS

SEMESTER 6

24SJHNECT601	ELECTRONIC DESIGN AUTOMATION	CATEGORY	L	T	P	CREDIT
		Honours	3	1	0	4

Preamble: The course aims to introduce principles behind advanced methods in automation of electronic design.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Outline VLSI design flow and design styles, and apply search, shortest path, and partitioning algorithms to solve graph-related problems.	K2
CO 2	Illustrate Design Layout Rules and apply different algorithms for layout compaction.	K2
CO 3	Apply various algorithms to solve placement and floorplan problems.	K3
CO 4	Apply different algorithms to solve routing problems.	K3

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PSO1	PSO2
CO1	3	3	2	1	1	-	-	-	-	-	2	2	-
CO2	3	3	2	1	1	-	-	-	-	-	2	2	-
CO3	3	3	2	1	1	-	-	-	-	-	2	2	-
CO4	3	3	2	1	1	-	-	-	-	-	2	2	-

Syllabus

Module I

Graph Terminology, Search Algorithms and Shortest Path Algorithms: Graph Terminology: Basic graph theory terminology, Data structures for representation of Graphs. Search Algorithms: Breadth First Search, Depth First Search, Topological Sort. Shortest Path Algorithms: Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path.
Design Automation and Partitioning Algorithms: Design Automation: VLSI Design Flow, VLSI Design Styles shortest path. Partitioning: Levels of Partitioning, Parameters for Partitioning, Classification of Partitioning Algorithms. Kernighan-Lin Algorithm, Simulated Annealing.

Module II

Layout Compaction: Layout: Layout Layers and Design Rules, Physical Design Optimizations.
Compaction: Applications of Compaction, Informal Problem Formulation, Graph Theoretical Formulation, Maximum Distance Constraints. Longest Path algorithm for DAG, Longest path in graph with cycles, Bellman-Ford Algorithm.

Module III

Placement and Floor planning: Placement: Optimization Objectives, Wirelength Estimation. Weighted Wirelength, Maximum Cut Size, Wire Density. Placement Algorithms: Quadratic Placement. Floor planning: Optimization Objectives, Slicing Floorplan, Non-Slicing Floorplan. Floorplan Representations: Constraint Graph, Sequence Pair. Floorplan Algorithms: Minimum Area Algorithm.

Module IV

Global Routing and Detailed Routing: Global Routing: Terminology and Definitions, Optimization Goals, Representation of Routing Regions. Maze Routing Algorithms: Lee's Algorithm, Hadlock Algorithm. Detailed Routing: Horizontal and Vertical Constraint Graph. Channel Routing Algorithms: Left-Edge algorithm.

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Text Books

1. Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011th edition.

2. Gerez,Sabih H., "Algorithms for VLSI Design Automation", John Wiley & Sons, 2006.

3. Sherwani, Naveed A., "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 1999.

Reference Books

1. Sadiq M. Sait and H. Youssef, "VLSI Physical Design Automation: Theory and ractice", World Scientific, 1999.

2. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "Introduction to Algorithms." The MIT Press, 3rd edition, 2009

SEMESTER 7

24SJHNECT701	RF MEMS	CATEGORY	L	T	P	CREDIT
		Honours	3	0	0	3

Preamble: This course introduces the principles, fabrication techniques and RF applications of MEMS-based switches, passive components, filters, and antennas used in modern wireless systems.
Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the fundamentals of MEMS technology, microfabrication processes, and actuation mechanisms used in RF MEMS.	K2
CO 2	Describe the structure, operation, and modelling of RF MEMS switches.	K3
CO 3	Analyze RF MEMS passive components such as inductors and capacitors with respect to layout, performance, and tunability.	K2
CO 4	Evaluate RF MEMS filters, phase shifters, and micromachined antennas for wireless and high-frequency applications.	K3

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PSO1	PSO2
CO1	3	2	-	-	2	-	-	-	-	-	1	2	-
CO2	2	3	-	3	2	-	-	-	-	-	1	-	-
CO3	2	3	-	2	2	-	-	-	-	-	1	2	-
CO4	1	2	2	-	2	-	-	-	2	2	1	-	-

Syllabus

Module I

Introduction: RF MEMS for wireless applications – MEMS technology and fabrication – Mechanical modeling of MEMS devices – MEMS materials and fabrication techniques: Surface micromachining, Bulk micromachining, LIGA –
Actuation Mechanisms in MEMS: Piezoelectric, Electrostatic, Thermal, Magnetic.

Module II

MEMS Switches: Introduction to RF MEMS switches – Capacitive shunt and series switches: Physical description, circuit model and electromagnetic modeling – Techniques of MEMS switch fabrication and packaging – Design considerations of RF MEMS switches.

Module III

Inductors and Capacitors: Micromachined passive elements – Micromachined inductors: Effect of inductor layout, reduction of stray capacitance of planar inductors, folded inductors, variable inductors and polymer-based inductors –
MEMS Capacitors: Gap-tuning capacitors, area-tuning capacitors, dielectric-tunable capacitors.

Module IV

RF Filters and Phase Shifters: Principle of operation of micromachined filters, surface acoustic wave (SAW) filters, micromachined filters for millimeter-wave frequencies – Various types of MEMS phase shifters – Ferroelectric phase shifters –
Micromachined Antennas: Micromachining techniques to improve antenna performance, reconfigurable antennas.

Course Assessment Method (CIE: 40 marks, ESE: 60 marks)

Text Books

1. Gabriel M. Rebeiz, "RF MEMS: Theory, Design, and Technology", Wiley, 2003.
2. Eun Sok Kim, "Fundamentals of Microelectromechanical Systems (MEMS)", McGraw Hill, 2006.
3. N. Maluf and K. Williams, "An Introduction to Microelectromechanical Systems Engineering", Artech House, 2004.
4. S. D. Senturia, "Microsystem Design", Springer, 2001.
5. S. K. Koul and S. Dey, "Micromachined Circuits and Devices: Microwave to Sub-Millimeter Applications", Springer, Singapore, 202

Reference Books

1. Sadiq V. K. Varadan, K. J. Vinoy and K. A. Jose, "RF MEMS and Their Applications", Wiley, 2003.
2. Hector J. De Los Santos, "RF MEMS Circuit Design for Wireless Applications", Artech House, 2002.
3. M. Madou, "Fundamentals of Microfabrication", CRC Press, 2002.
4. N. P. Mahalik, "Microsensors and MEMS", Springer, 2007.