CURRICULUM & SYLLABUS

B. Tech. (Honours)

ELECTRONICS AND COMPUTER ENGINEERING (ER)

2024 SCHEME

CURRICULUM

B.Tech. (Honours) is an enhanced version of the Bachelor of Technology degree, offering the students the opportunity to undertake additional courses within their own discipline. This pathway allows students to deepen their knowledge in emerging or advanced areas of Engineering relevant to their field of study, providing a stronger foundation for specialized career paths or further academic pursuits.

For the award of B.Tech. (Honours) in Electronics and Computer Engineering, the student shall fulfill all the curricular requirements for B.Tech. in Electronics and Computer Engineering as per SJCET B.Tech. Academic Regulations 2024 and shall earn 15 additional credits by undergoing the following courses, which shall be further governed by clause R16 of the Regulations.

Sl. No.	Semester	Course Code	Course Name/Type	Weekly hours				Total Marks		Credits
				L	T	P	SS	CIE	ESE	
1	4	24SJHNERT409	Advanced Digital System Design	3	1	0	5	40	60	4
2	5	24SJHNERT509	Nanoelectronics	3	1	0	5	40	60	4
		24SJHNERM5XX	Approved MOOC *							
3	6	24SJHNERT609	Electronic Design and Automation Tools	3	1	0	5	40	60	4
		24SJHNERM6XX	Approved MOOC *							
4	7	24SJHNERT709	Digital System Design Using VHDL	3	0	0	5	40	60	3
		24SJHNERM7XX	Approved MOOC *							
Total Credits										15

*MOOC to be approved by the Academic Council on recommendation of the Board of Studies.

SEMESTER: S4 (Honours)

ADVANCED DIGITAL SYSTEM DESIGN

Course Code	**24SJHNERT 409**	**CIE Marks**	40
Teaching Hours/Week (L:T:P:R)	3:1:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs 30 Mins
Prerequisites (if any)	PCERT 303: Digital System Design Using Verilog	**Course Type**	Theory

Course objectives:

- To equip students with the knowledge of combinational circuit design, programmable logic devices, and hierarchical digital system design using Verilog HDL.
- To introduce FPGA-based digital system design methodologies, including high-level architecture, floor planning, and physical design strategies.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Combinational Circuit Design and Programmable Logic Devices: Combinational circuit implementation using Quine Mc Cluskey algorithm. Programmable logic Devices -ROM, PLA, PAL, CPLD, FPGA Features. Implementation using ROM, PLA and PAL, Multi output gate implementation.	**11**
2	Hierarchical Digital System Design and Verilog Implementation: Digital System Design Hierarchy - state assignments, reduction of state tables, equivalent states, determination of state equivalence using implication table. Algorithm state machine, ASM charts, Design example. Verilog HDL implementation of binary multiplier, divider, barrel shifter, FSM, linear feedback shift register	**11**
3	Fundamentals of FPGA-Based Digital System Design: Digital system design options and trade-offs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modelling and simulation, Hardware description languages (emphasis on Verilog), combinational and sequential design, state machine design, synthesis issues, test benches.	**11**
4	FPGA Floor planning and Physical Design Strategies: Floor planning Methods – Chip-level physical design, Block placement & channel definition, Global routing, Switchbox routing. Global interconnect – Interconnect properties & wiring plans, power distribution, clock distribution. Floorplan design – floor planning tips, design validation. Off-chip connections – packages, I/O architecture, pad design.	**11**

Course Assessment Method

(CIE: 40 Marks, ESE: 60 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	*Assignment/Micro project*	*Internal Ex-1*	*Internal Ex-2*	*Total*
10	**10**	**10**	**10**	**40**

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course the student will be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Design simple digital systems with programmable logic devices	K3
CO2	Develop hierarchical digital systems and implement complex logic functions using Verilog HDL.	K3
CO3	Explain FPGA-based digital system design methodologies and high-level architecture specific	K2
CO4	Describe FPGA floor planning methods and physical design strategies	K2

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table:

Course Articulation Matrix (Mapping of course outcomes with program outcomes)**:**

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	2	-	1	-	-	-	-	-	2
CO2	3	3	2	-	3	-	-	-	-	-	2
CO3	3	2	-	-	1	-	-	-	-	-	3
CO4	3	2	-	-	1	-	-	-	-	-	3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Textbooks				
SL No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Fundamentals of Logic Design	Charles H. Roth	Thomson Press (India) Ltd	5th Edition, 2004
2	FPGA-Based System Design	Wayne Wolf, Verlag	Prentice Hall	2004
3	Modern VLSI Design: System-on-Chip Design	Wayne Wolf, Verlag	Pearson Education	3rd Edition
4	Field-Programmable Gate Arrays	Stephen D. Brown	Springer	1st Edition, 2012

Reference Books				
1	Fundamentals of Digital Logic with Verilog HDL	S Brown & Z. Varanestic	Mc Graw Hill	3rd Edition, 2023
2	Verilog HDL a guide to digital design & synthesis	Samir Palitkar	Pearson	2nd Edition, 2001
3	Digital Principles of Design	Donald D Givone,	McGraw Hill	2003
4	Field Programmable Gate Array Technology	S. Trimberger	Kluwer Academic	1994
5	Introduction to digital systems	Milos D. Ercegovac	John Wiley Sons	1st Edition, 1998

Video Links (NPTEL, SWAYAM etc):	
Module - I	NPTEL : Electrical Engineering - NOC: Digital System Design, Prof. Neeraj Goel, IIT Ropar, Lecture 31 Digital System Design (Prof. Neeraj Goel, IIT Ropar): Lecture 31 - Programmable Hardware
Module - II	NPTEL : Electrical Engineering - NOC: Digital System Design, Prof. Neeraj Goel, IIT Ropar, Lecture 21 Digital System Design (Prof. Neeraj Goel, IIT Ropar): Lecture 21 - Verilog Simulation Demo
Module - III	NPTEL : Electrical Engineering - NOC: Digital System Design, Prof. Neeraj Goel, IIT Ropar, Lecture 66 Digital System Design (Prof. Neeraj Goel, IIT Ropar): Lecture 66 - Xilinx CLB
Module - IV	NPTEL : Electrical Engineering - NOC: Digital System Design, Prof. Neeraj Goel, IIT Ropar, Lecture 67 Digital System Design (Prof. Neeraj Goel, IIT Ropar): Lecture 67 - FPGA Design Flow

SEMESTER S5 (Honours)
NANOELECTRONICS

Course Code	24SJHNERT509	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs 30 Mins
Prerequisites (if any)	24SJGBPHT121 - Physics for Electrical Science 24SJPBERT304 - Electronic Devices and Circuits	Course Type	Theory

Course Objectives:

1. To impart fundamental knowledge of quantum mechanical principles and the behaviour of materials at the nanoscale.
2. To enable students to understand the fabrication, transport, characterization, and device operation aspects of nanoelectronic systems.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Fundamentals of Nanoelectronics:** Introduction to nanotechnology, Limitations of conventional microelectronics, characteristic lengths in mesoscopic systems, Classification of materials based on electrical properties: conductors, insulators, and semiconductors, Concept of energy bands and carrier behaviour in semiconductors. Low dimensional structures - Quantum wells, wires and dots, Density of states of 1D and 2D nanostructures.	11
2	**Fabrication of Nanomaterials and Nanostructures:** Introduction to methods of fabrication of nano-layers: physical vapour deposition-evaporation & Sputtering, Chemical vapour deposition, Molecular Beam Epitaxy, Ion Implantation, Formation of Silicon Dioxide- dry and wet oxidation methods. Fabrication of nano particle- grinding with iron balls, laser ablation, reduction methods, sol gel, self-assembly, precipitation of quantum dots.	11

3	**Quantum Transport and Electronic Phenomena in Nanostructures:** Quantum wells, multiple quantum wells, Modulation doped quantum wells, Basic properties of square quantum wells of finite depth, parabolic and triangular quantum wells Transport of charge in Nanostructures - Electron scattering mechanisms, Hot electrons, Resonant tunnelling transport, Coulomb blockade, Effect of magnetic field on a crystal. Aharonov-Bohm effect.	**11**
4	**Characterization Techniques and Nanoelectronic Devices:** Introduction to characterization of nanostructures: Principle of operation of Scanning Tunnelling Microscope, Atomic Force Microscope, Scanning Electron microscope - specimen interaction, Xray Diffraction analysis. Nanoelectonic devices - MODFETS, FinFET, Single Electron Transistor, CNT transistors	**11**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
10	**10**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 = 24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain the transition in electrical and quantum mechanical behaviour of materials from bulk semiconductors to low-dimensional nanostructures.	K2
CO2	Describe the different processes involved in the fabrication of nanoparticles and nanolayers.	K2
CO3	Explain the mechanisms of charge transport and the influence of quantum effects on electronic behaviour in nanostructures.	K2
CO4	Illustrate the operating principles of nanoscale electronic devices and explain the techniques used for characterizing nano layers and particles.	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

Course Articulation Matrix (Mapping of course outcomes with program outcomes):

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	-	-	-	-	-	-	-	-	1
CO2	3	2	1	-	-	-	-	-	-	-	1
CO3	3	3	-	-	-	-	-	-	-	-	1
CO4	3	2	1	1	-	-	-	-	-	-	2

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No.	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Nanotechnology for Microelectronics and optoelectronics	J.M. Martinez-Duart, R.J. Martin Palma, F. Agulle Rueda	Elsevier	2nd Edition, 2017
2	Nanotechnology and Nanoelctronics	W.R. Fahrner	Springer	2005

Reference Books				
Sl. No.	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to Nanoscience & Technology	Chattopadhyay, Banerjee	PHI	2012
2	Introduction to Nanotechnology	Poole	John Wiley	2006
3	Fundamentals of Nanoelectronics,	George W. Hanson	Pearson Education	2009
4	Nanoelectronics and nanosystems	K. Goser, P. Glosekotter, J. Dienstuhl	Springer	2013
5	Quantum Transport- Atom to transistor	Supriyo Dutta	Cambridge	2013

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	NPTEL: Nanoelectronics: Devices and Materials, IISc Bangalore, Dr. Navakanta Bhat, Dr. S.A. Shivashankar, Prof. K.N. Bhat, Lecture Name: Introduction to Nanoelectronics nptel.ac.in/courses/117108047
2	NPTEL: Nanoelectronics: Devices and Materials, IISc Bangalore, Dr. Navakanta Bhat, Dr. S.A. Shivashankar, Prof. K.N. Bhat, Lecture Name: Chemical vapour deposition (CVD) and atomic layer deposition (ALD) nptel.ac.in/courses/117108047
3	NPTEL: Nanoelectronics: Devices and Materials, IISc Bangalore, Dr. Navakanta Bhat, Dr. S.A. Shivashankar, Prof. K.N. Bhat, Lecture Name: Basic Principles of Quantum Mechanics nptel.ac.in/courses/117108047
4	NPTEL: Nanoelectronics: Devices and Materials, IISc Bangalore, Dr. Navakanta Bhat, Dr. S.A. Shivashankar, Prof. K.N. Bhat, Lecture Name: Quantum structures and devices nptel.ac.in/courses/117108047

SEMESTER S6 (Honours)

ELECTRONIC DESIGN AND AUTOMATION TOOLS

Course Code	**24SJHNERT609**	**CIE Marks**	**40**
Teaching Hours/Week (L: T:P: R)	3:1:0:0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs 30 Mins
Prerequisites (if any)	24SJPCERT205 - DIGITAL ELECTRONICS	**Course Type**	Theory

Course Objectives:

1. To understand the complete Electronic Design Automation flow encompassing design methodologies, synthesis, verification, and simulation techniques used in modern VLSI system design
2. To familiarize students with library and geometric layout design, assembly and packaging methods, PCB design flow, and design-for-testability principles for reliable electronic system implementation.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Concept of EDA:** Design Methodology, Development steps, Implementation and Verification, Top Down or Bottom Up, Short history of EDA. Digital Simulation: Why? Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation.	**11**
2	**Synthesis:** Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping. Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification.	**11**
3	**Library Design:** Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries. ASICs: Design goals for ASICs, Design Styles. Geometric layout: Standard cell Layouts, LEF data format, GDSII format. Geometric Verification: Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS.	**11**

4	**Assembly, Packaging, and Testability in Electronic Design:** Die Assembly, Electrical connections, Packaging Methods. PCB Design: PCB design flow, Schematic entry for PCB design, PCB layout. Design for Testability Fundamentals: Role of testing, Digital & analog VLSI testing, VLSI Technology trends affecting Testing, how to test chips, types of testing, Automatic test equipment.	**11**

Course Assessment Method

(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Illustrate the basic concepts of EDA, fault simulation and testability	K2
CO2	Understand partitioning and formal verification techniques	K2
CO3	Describe the need for library design, ASICs and geometric verification	K2
CO4	Explain the principles of assembly, packaging methods, PCB design flow, and fundamentals of testability in electronic and VLSI systems	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

Course Articulation Matrix (Mapping of course outcomes with program outcomes):

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	1	-	-	-	-	-	-	-	2
CO2	3	2	1	-	-	-	-	-	-	-	2
CO3	3	2	1	-	-	-	-	-	-	-	2
CO4	3	2	1	-	-	-	-	-	-	-	2

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No.	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	The Electronic Design Automation Handbook	Dirk Jansen	Springer	2010
2	Digital Systems Testing and Testable Design	Miron Abramovici, Melvin A. Breur, Arthur D. Friedman	Jaico Publishing House	4th Edition, 2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	M.J.S.Smith	Application-Specific Integrated Circuits	Pearson	2010
2	Jan M. Rabaey, A. Chandrakasan, B. Nikolic	Digital Integrated Circuits: A Design perspective	Pearson	2017
3	M.H.Rashid	SPICE For Circuits and Electronics Using PSPICE	Prentice Hall	2nd edition, 2011
4	Vishwani Agrawal, M. Bushnell	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	Springer	2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	NPTEL: Digital Design with Verilog by Prof. Chandan Karfa, Prof. Aryabartta Sahu - IIT Guwahati: Lec 41 - Introduction to Electronic Design Automation (https://onlinecourses.nptel.ac.in/noc24_cs61/preview)
2	NPTEL: Optimization Techniques for Digital VLSI Design, IIT Guwahati by Prof. Chandan Karfa, Prof. Santosh Biswas – Lecture Name: Introduction to Digital VLSI Design Flow (https://nptel.ac.in/courses/108103108?utm_source)
3	NPTEL: VLSI Design Verification and Test, IIT Guwahati by Prof. Jatindra Kumar Deka, Dr. Santosh Biswas – Lecture Name: Introduction to Digital VLSI Design Flow (https://nptel.ac.in/courses/106103016?utm_source)
4	NPTEL: VLSI Design Verification and Test, IIT Guwahati by Prof. Jatindra Kumar Deka, Dr. Santosh Biswas, Module 8: Fault Simulation and Testability Measures - Lecture name: Fault Simulation (https://nptel.ac.in/courses/106103016?utm_source)