



ST. JOSEPH'S
COLLEGE OF ENGINEERING
AND TECHNOLOGY,
- PALAI -
AUTONOMOUS

Choondacherry P.O., Pala, Kottayam - 686579
Kerala, India



CURRICULUM & SYLLABUS

B. Tech. (Honours)

ELECTRONICS AND COMPUTER ENGINEERING (ER)
2024 SCHEME

www.sjcetpalai.ac.in



Signed By: DEVASSIA V P
Approved by Academic
Council dtd.19.06.2026

CURRICULUM

B.Tech. (Honours) is an enhanced version of the Bachelor of Technology degree, offering the students the opportunity to undertake additional courses within their own discipline. This pathway allows students to deepen their knowledge in emerging or advanced areas of Engineering relevant to their field of study, providing a stronger foundation for specialized career paths or further academic pursuits.

For the award of B.Tech. (Honours) in Electronics and Computer Engineering, the student shall fulfill all the curricular requirements for B.Tech. in Electronics and Computer Engineering as per SJ CET B.Tech. Academic Regulations 2024 and shall earn 15 additional credits by undergoing the following courses, which shall be further governed by clause R16 of the Regulations.

Sl. No.	Semester	Course Code	Course Name/Type	Weekly hours				Total Marks		Credits
				L	T	P	SS	CIE	ESE	
1	4	24SJHNERT409	Advanced Digital System Design	3	1	0	5	40	60	4
2	5	24SJHNERT509	Nanoelectronics	3	1	0	5	40	60	4
		24SJHNERM5XX	Approved MOOC *							
3	6	24SJHNERT609	Electronic Design and Automation Tools	3	1	0	5	40	60	4
		24SJHNERM6XX	Approved MOOC *							
4	7	24SJHNERT709	Digital System Design Using VHDL	3	0	0	5	40	60	3
		24SJHNERM7XX	Approved MOOC *							
Total Credits										15

*MOOC to be approved by the Academic Council on recommendation of the Board of Studies.



SEMESTER S7
DIGITAL SYSTEM DESIGN USING VHDL

Course Code	24SJHNERT709	CIE Marks	40
Teaching Hours/Week (L:T:P:R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	24SJPCERT205 - Digital Electronics	Course Type	Theory

Course Objectives:

1. To explain VHDL constructs and modeling styles (behavioral, dataflow, and structural) for representing digital systems.
2. To apply VHDL-based design techniques for developing and verifying combinational and sequential circuits, including finite state machines, using testbenches.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to VHDL: What is VHDL, Capabilities, Hardware Abstraction, Basic Terminology, Entity Declaration, Architecture Body, Structural Style of Modeling, Dataflow Style of Modeling, Behavioral Style of Modeling, Mixed Style of Modeling, Configuration Declaration, Package Declaration, Package Body, Model Analysis. Basic Language Elements – Identifiers, Data Objects, Data Types: Subtypes, Scalar Types, Composite Types, Lexical conventions. Operators: Logical Operators, Relational Operators, Adding Operators, Multiplying Operators.	9
2	Behavioral and Dataflow Modeling using VHDL: Behavioral Modeling: Process statement, Sequential statements: variable and signal assignment statements, wait statement, if statement, case statement, null statement, loop and next statements, assertion statement. Signal assignment concepts: inertial delay model, transport delay model, signal drivers, multiple processes. Dataflow Modeling: Concurrent signal assignment statements, conditional and selected signal assignment statements, concurrent vs sequential execution, delta delay, multiple drivers, block statement,	9



	concurrent assertions.	
3	Structural Modeling and Combinational Circuit Design using VHDL: Structural Modeling: Component declaration and instantiation, resolving signal values. Combinational Circuit Design using VHDL: Adder, Difference circuit Multiplexer, Demultiplexer, Decoder, Encoder, 3-bit comparator, BCD to 7-Segment Decoder, Addition-subtraction circuit, Four-Bit Full Adder, Binary Multiplier. Testbenches for structural & combinational circuits.	9
4	Sequential Circuit Design using VHDL: Flip flop design using VHDL, Counters: Binary counter, Decade counter, Programmable mod-n counter, Ring counter, Decimal counter, Synchronous Up/Down Counter. Shift register: Free-running shift-right register, Universal shift register. Finite State Machine Design Using VHDL – Mealy & Moore (overlapping , non-overlapping, one-hot encoding for FSMs). Testbenches for sequential circuits.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
10	10	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
2 Questions from each module. - Total of 8 Questions, each carrying 3 marks (8x3 =24marks)	- Each question carries 9 marks. - Two questions will be given from each module, out of which 1 question should be answered. - Each question can have a maximum of 3 sub divisions. (4x9 = 36 marks)	60



Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Explain VHDL constructs, data types, and modeling styles for representing digital systems at different levels of abstraction.	K2
CO2	Describe behavioral and dataflow modeling techniques used in VHDL.	K2
CO3	Apply structural modeling techniques and implement combinational digital circuits using various modeling styles in VHDL, and test their functionality using testbenches.	K3
CO4	Apply VHDL concepts to design and implement sequential circuits and finite state machines, and verify their operation using testbenches.	K3

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	2	3	1
CO2	2	1	-	-	-	-	-	-	-	-	2	3	1
CO3	3	2	2	1	1	-	-	-	-	-	2	3	1
CO4	3	2	2	1	1	-	-	-	-	-	2	3	1

Note: 1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	VHDL Primer	J. Bhasker	Paperback	Third Edition, 2015
2	Free Range VHDL	Bryan Mealy, Fabrizio Tappero	Free Range Factory	2013
3	RTL Hardware Design Using VHDL	Pong P Chu	John Wiley & Sons	2006
4	Fundamentals of Logic Design	Charles H Roth	Stamford	7 th edition, 2014



Reference Books				
Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Digital System Design with VHDL	Mark Zwolinski	Pearson Education	Second Edition, 2007
2	Digital Design Principles and Practices	John F Wakerly	Pearson Education	2002
3	Digital Design	Morris Mano,	Pearson Education,	2002

Video Links (NPTEL, SWAYAM...)	
Module No.	Link ID
1	NPTEL Course: Digital Circuits by Prof. Santanu Chattopadhyay, Lecture 46 - VHDL NPTEL Video Link
2	NPTEL Course: Advanced VLSI Design by Prof. A.N. Chandorkar, Prof. D.K. Sharma, Prof. Sachin Patkar, Prof. Virendra Singh. Mod-01 Lec-22 Behavioral Description in VHDL NPTEL Video Link
3	NPTEL Course: Advanced VLSI Design by Prof. A.N. Chandorkar, Prof. D.K. Sharma, Prof. Sachin Patkar, Prof. Virendra Singh. Mod-01 Lec-21 Structural Description in VHDL NPTEL Video Link
4	NPTEL Course: Synthesis of Digital Systems by Prof. Preeti Ranjan Panda, Lecture Name: Finite State Machine Synthesis: Introduction to FSM Encoding NPTEL Video Link

